# ATARI®

# 1050™ DISK DRIVE

# FIELD SERVICE MANUAL

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## INTRODUCTION

The Atari 1050™ Disk Drive Field Service Manual is a reference guide for you, the service technician. The information presented in this manual, when used in conjunction with Atari training enables you to repair and maintain Atari 1050 Disk Drive units.

This Field Service Manual is organized in seven sections:

- **THEORY OF OPERATION** - Overview of how the 1050 Disk Drive works and what its basic assemblies look like.
- **TEST EQUIPMENT/DIAGNOSTIC TESTS** - Review of all Diagnostic Tests available for diagnosing 810 Disk Drive problems.
- **DISASSEMBLY/ASSEMBLY** - Detailed procedures for disassembling and assembling the 1050 Disk Drive.
- **SYMPTOM CHECKLIST** - Failure information to assist the experienced technician arrive at a rapid diagnosis of 1050 Disk Drive problems.
- **ASSEMBLY DRAWINGS AND PARTS LIST** - Detailed breakdown of all parts used in the 1050 Disk Drive.
- **APPENDIX A** - Contains 1050 mechanical and electrical specifications.
- **SERVICE BULLETINS** - Section to be used to hold Field Change Orders, Upgrade Bulletins and Tech Tips.

# SECTION 1

# THEORY OF OPERATION

## OVERVIEW

The ATARI 1050 Disk Drive is a record/playback device that allows information to be stored and retrieved quickly and accurately. The actual recording is much like a tape recording process and is done on similar material. The data is magnetically recorded on a 5 1/4 inch diameter diskette. Each diskette can store 88K bytes of data in single density mode and 133K bytes in double density however, double density can only be implemented in conjunction with DOS3. The diskette is inserted through a door in the front panel of the drive unit. The 1050 Disk Drive is used with a single ATARI 400, 800 or 1200 Computer with a minimum of 16K of RAM installed.

Figure 1-1 is a simplified block diagram of the functional flow of the 1050 follows. Each of its functional units are explained in greater detail below.

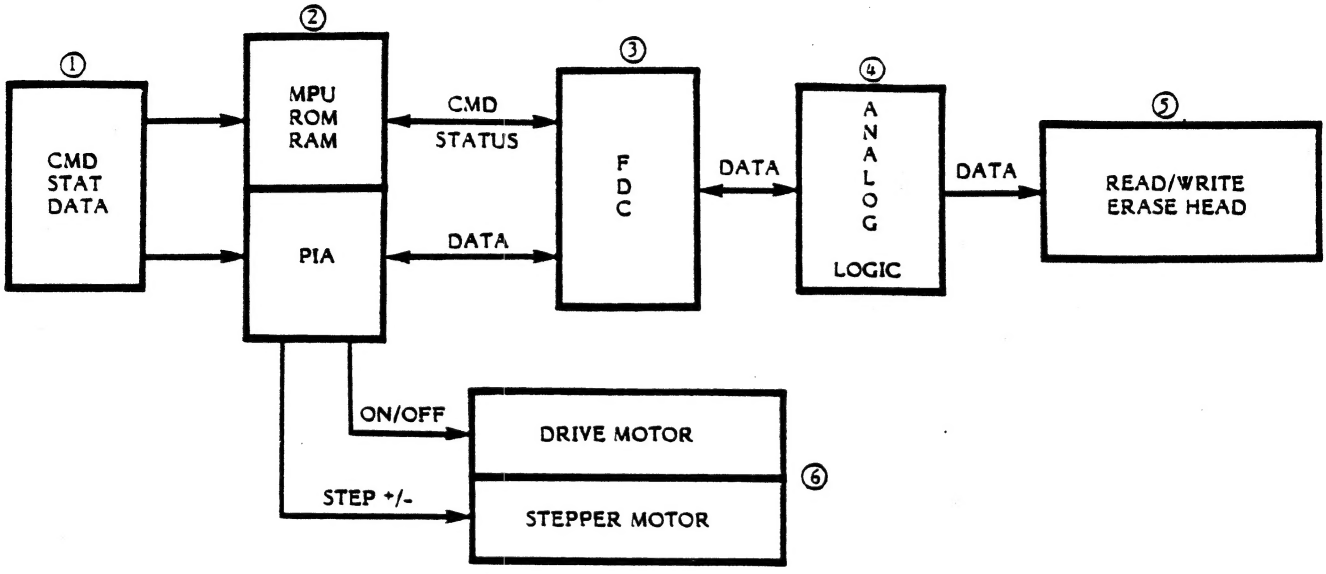



Figure 1-1. Simplified Block Diagram

Block 1 includes the Data Input/Output (I/O) connectors. They are the origin and destination of all commands, status and data.

Block 2 includes the Microprocessor (MPU), Read-Only-Memory (ROM), Random-Access-Memory (RAM) and Peripheral Interface Adaptor (PIA). They process all commands and control data flow to and from the console.

Block 3 includes the 2793 Floppy Disk Controller (FDC). The FDC controls data flow to and from the diskette.

Block 4 includes the Analog Logic. The Analog Logic processes all data to and from the Read/Write Head.

Block 5 includes the Read/Write and Erase Head.

Block 6 includes the Stepper Motor and Drive Motor which are located in the Drive Mechanism. They receive signals from the PIA.

## OPERATOR FUNCTIONS

Each 1050 Disk Drive comes with an AC Power Adaptor and a Data Cord. Figure 1-2 shows how to connect the Disk Drive and computer console.

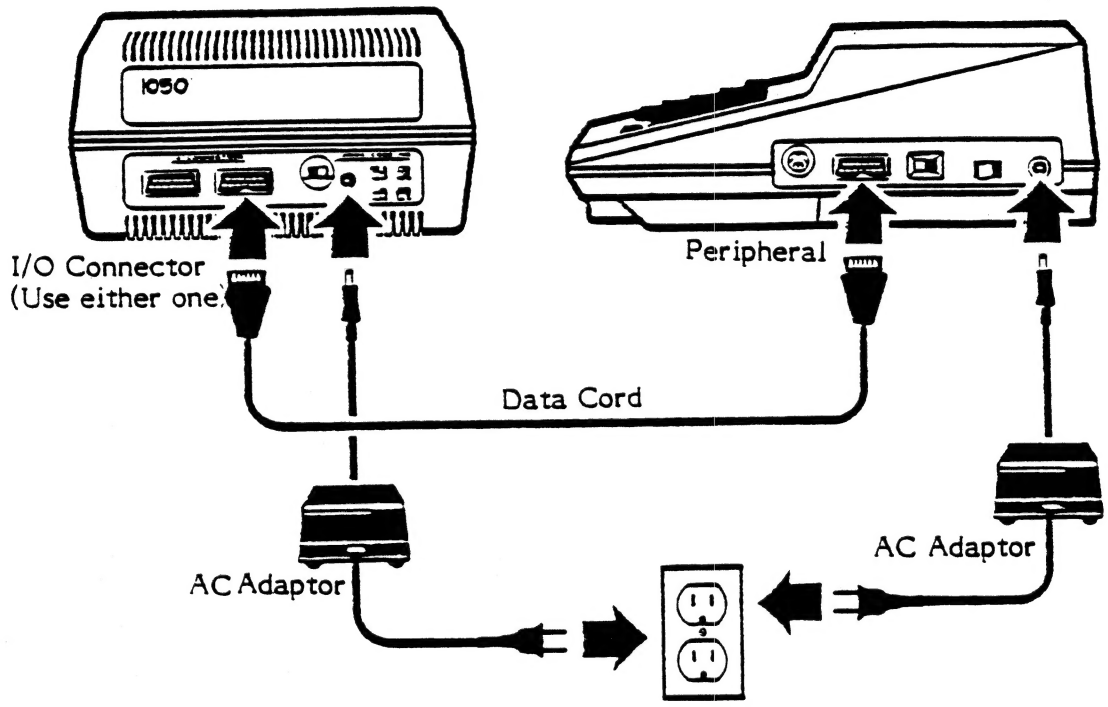
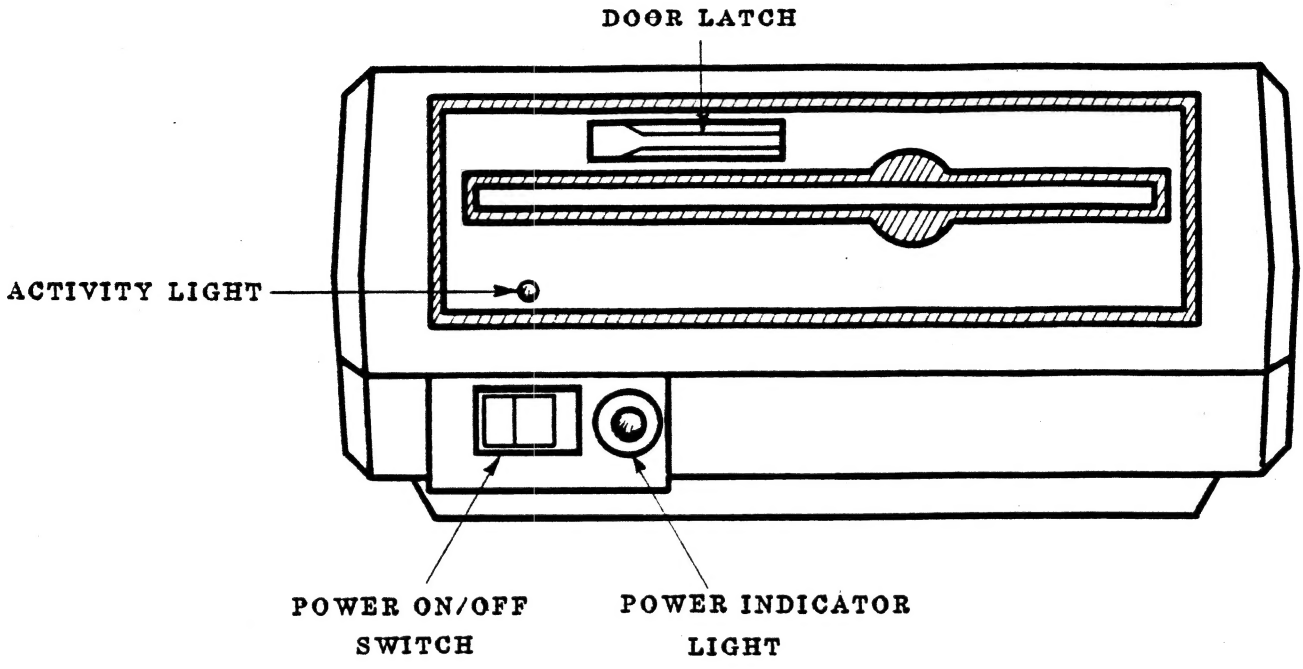



Figure 1-2. System Hook-up

The Controls/Indicators are located on the front and back panels of the 1050. The front panel of the 1050 contains the Activity Light, the Power Indicator Light, the Power ON/OFF switch, and the door latch. The rear panel of the 1050 contains the Input/Output (I/O) connectors, Power-Jack, and Drive Code Switch. (Use Atari 810 switch settings to identify drive as number 1,2,3, or 4.).

These functions are illustrated in Figure 1-3 and discussed in the following paragraphs.

FRONT PANEL




BACK PANEL

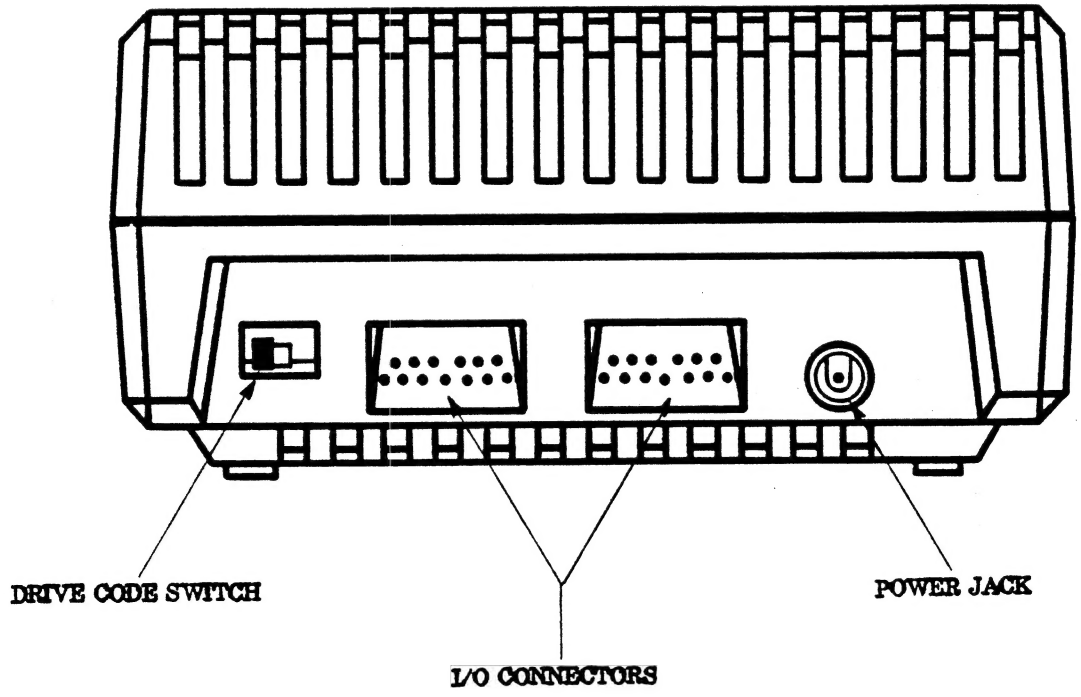



Figure 1-3. ATARI 1050 Disk Drive Control/Indicators

## Front Panel

The Activity Light lights whenever the drive is reading from or writing to a diskette or when the diskette is first inserted and the door latch turned down. **DO NOT OPEN THE DRIVE DOOR, TURN POWER OFF, OR ATTEMPT TO REMOVE THE DISKETTE WHEN THIS LIGHT IS ON!**

The Power Indicator Light lights whenever power to the Drive is **ON.**

The Power ON/OFF switch is a toggle switch pushed to the right for **ON,** and to the left for **OFF. ALWAYS insert or remove a diskette with Power ON.**

The Door Latch turns down to close the door after a diskette is inserted. The Activity Light then lights for a few seconds. The latch turns parallel to the diskette slot for removing the diskette.

## Back Panel

The Input Output (I/O) connectors are identical jacks for the data cords from the computer console or other peripheral devices. Connections may be made in any order with either jack.

The Power Jack accepts the AC Power Adaptor.

The Drive Code Switch is a 4-position switch that tells the computer which drive it is communicating with.

Two switches (one black and one white) are visible in the rectangular opening on the drive rear panel. Using a pen or screwdriver, move the switches to the correct position on each drive being used.

Drive Code Number Diagram shows the correct positions of the Drive Code Switch to set the identification of the Drive (1 thru 4).

## MECHANICAL THEORY

The 1050 unit is composed of an outer case which houses the Drive Mechanism, Drive Motor, Head Carriage Assembly, Stepper Motor, and PCB.

### CASE

The 1050 outer case consists of three pieces of plastic. The lower cover secures the PCB and drive mechanism. The top cover protects these, as illustrated in Figure 1-4. The front bezel houses the Power and Activity lights, door latch, Power ON/OFF switch and diskette slot.

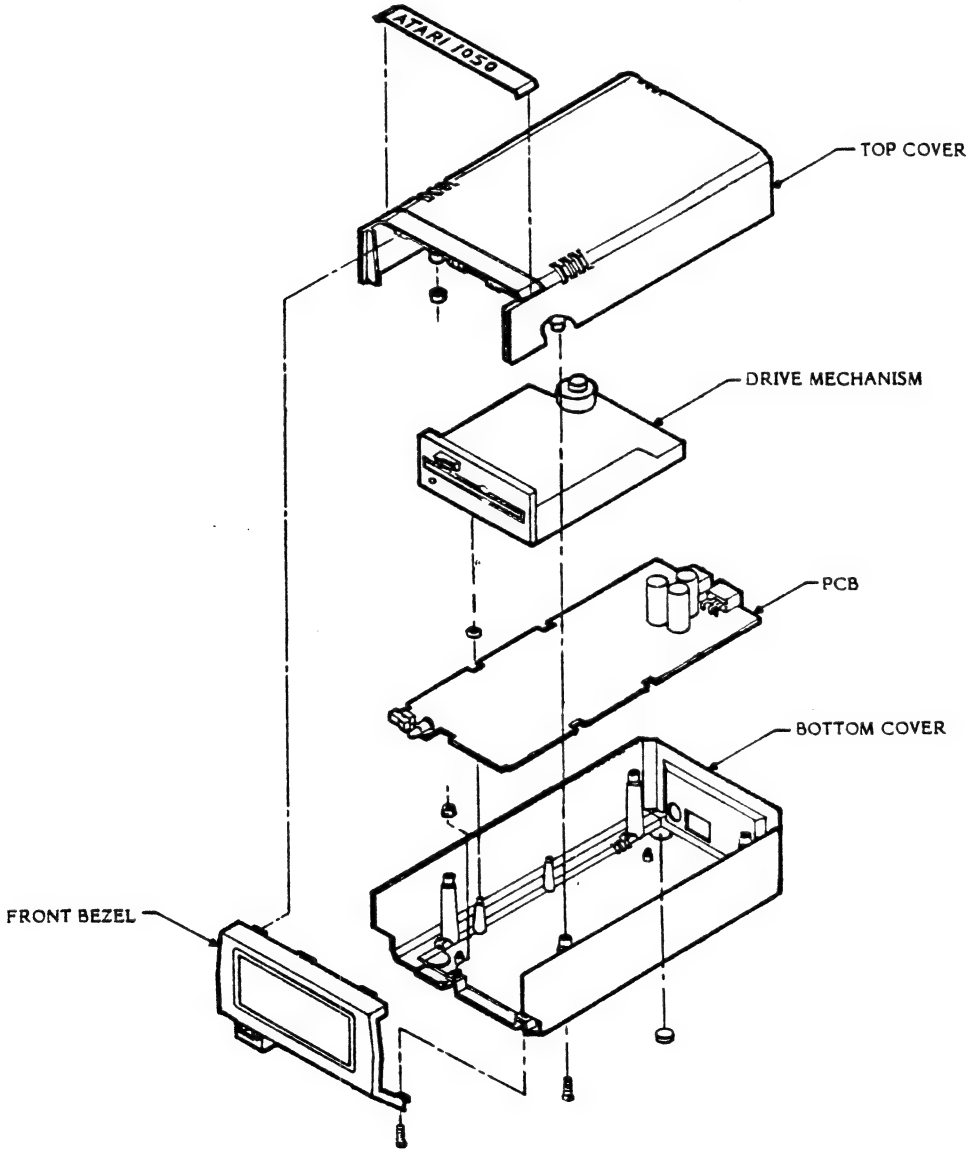



Figure 1-4. Exploded Diagram of the Disk Drive

Figure 1-4 illustrates the mechanical elements of the 1050 which are discussed in the following paragraphs.

## DRIVE MECHANISM

The Drive Mechanism provides mechanical and electronic linkage to the diskette. It is the physical assembly containing the Head Carriage Assembly, Drive Motor, Stepper Motor, and Write Protect sensor, Track 00 sensor, and Diskette Enable switch.

## HEAD CARRIAGE ASSEMBLY

The Head Carriage Assembly allows the head to be cycled across the diskette. It contains the Read/Write and Erase Head, the pressure pad and spring assembly.

## DRIVE MOTOR

The Drive Motor is a DC motor which indirectly drives the diskette. It is attached by a drive belt to a flywheel which rotates the disk.

The DC motor includes an internal Tachometer, whose output is monitored in the Tach Feedback circuit. The Tach Feedback circuit senses changes in current and maintains a constant motor speed.

The Activity Light (LED) comes on whenever the motor turns on.

## STEPPER MOTOR

The Stepper Motor positions the head over a desired track. It is a four-phase motor. Each change in phase rotates the Stepper Motor shaft. This circular motion is converted to linear motion by the positioning band/pulley assembly which links it to the head carriage.

The Stepper Logic is controlled by the PIA Chip. Four PIA signals act as the Stepper Motor's four-phase inputs. These lines in various combinations, drive the Stepper Motor to reposition the Head Carriage Assembly from track to track.

## PCB ASSEMBLY

All of the digital and analog logic for the 1050 is contained on one PCB.

## POWER SUPPLY

The Power Supply provides the following voltages for use in the system:

+5VDC (regulated), which provides the voltage for the logic and for the 2793-02 Floppy Disk Controller.

+12VDC (regulated), which feeds the Stepper Motor, Drive Motor, Zero Crossing Detector, Read/Write and Erase circuitry, and Tach feedback.

The 120VAC which comes into the system is stepped down to 9VAC by an external transformer (See Figure 1-6).

The 9VAC is applied to the bridge rectifier on the PCB when the Power ON/OFF switch is turned ON. An internal 2 amp fuse in the AC adaptor provides current limiting protection.

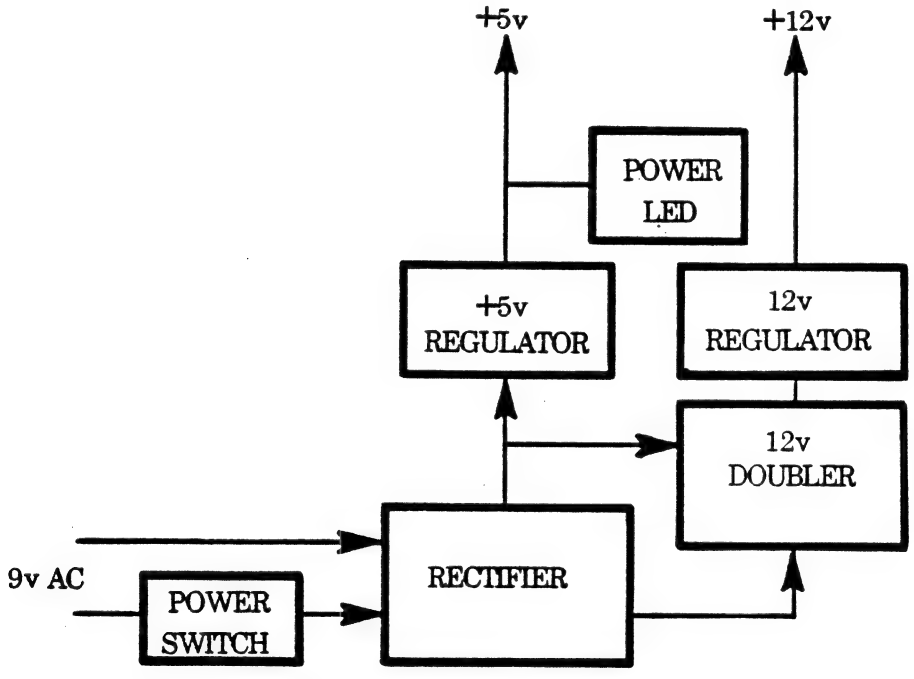



Figure 1-5. Power Supply Block Diagram

## POWER-UP LOGIC

The Disk Drive's Power-up Logic resets the 6507 microprocessor, Stepper Motor logic, Peripheral Interface Adaptor (PIA) and Data Interface section (2793 FDC and Analog circuitry) whenever the drive is turned on. In addition, the power-up logic circuit locks the Data Output Buffer off during the short period when the drive is turned on. This prevents random pulses generated by the drive's circuitry (during the initialization period) from being sent to the console.

The RESET logic returns the electrical circuits to their starting conditions.

## ELECTRONIC THEORY

The 1050 Disk Drive consists of eight major electronic elements. These include:

- Power-up Logic (discussed in the Power Supply section above)
- Clock
- 6507 Microprocessor Unit (MPU)
- Read-Only Memory (ROM)
- Random Access Memory (RAM)
- 6532 Peripheral Interface Adaptor (PIA)
- 2793 Floppy Disk Controller (FDC)
- Read/Write and Erase Logic

A functional block diagram of the electronic elements of the 1050 Disk Drive follows (Figure 1-6), along with a discussion of each.

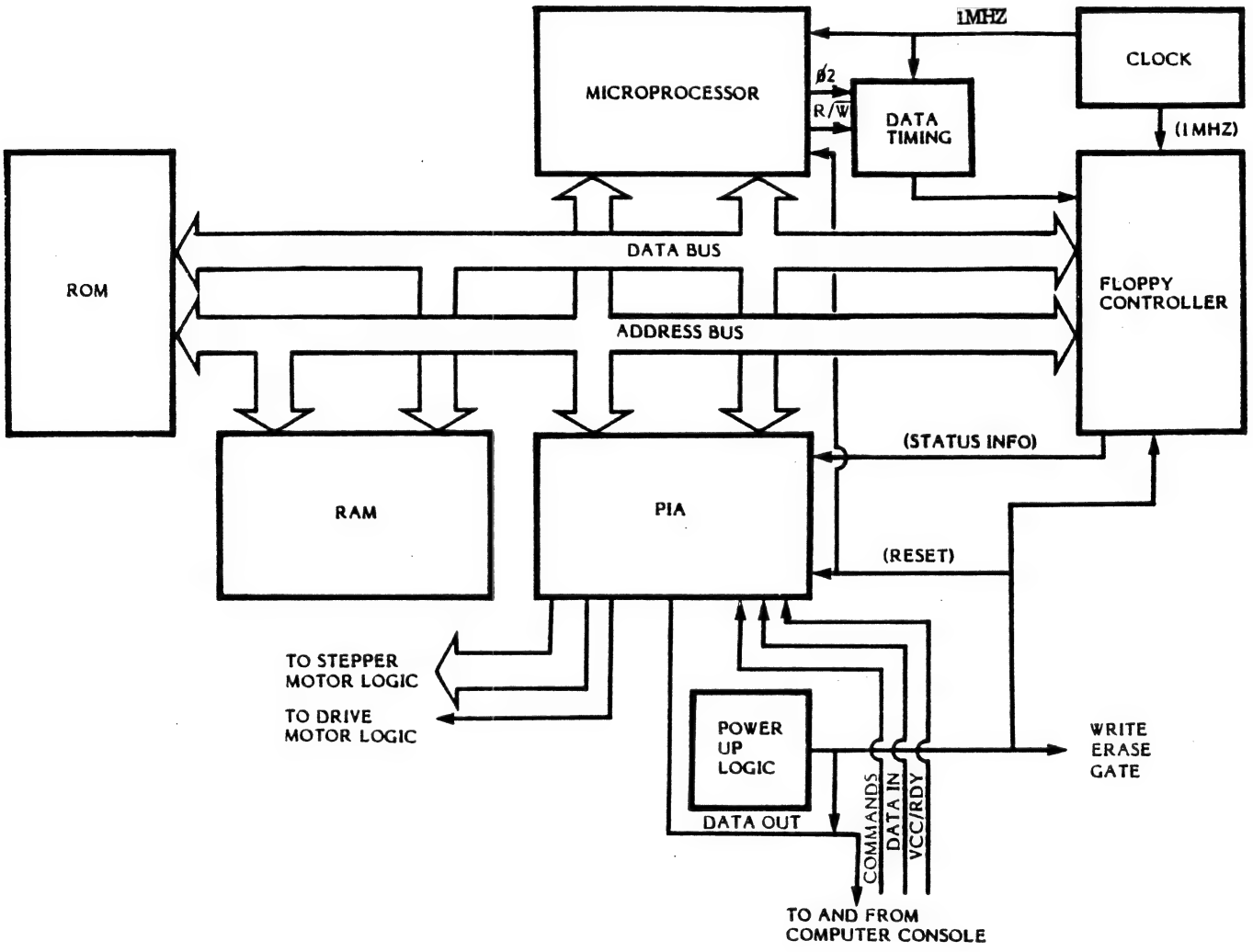



Figure 1-6. Disk Drive Electronic Units

## CLOCK

The clock generator produces a continuous waveform that controls all signal transitions in the system. It provides timing controls for the 1050 Disk Drive Logic and the Read/Write operations to the diskette.

The drive's clock circuitry generates a crystal controlled 1 MHz signal. The 1 MHz signal is used by the 2793 Floppy Disk Controller (FDC) and Write/Erase gate for timing serial data to the heads. It is also used by the 6507 microprocessor to clock parallel data into and out of the FDC.

## 6507 MICROPROCESSOR

The Disk Drive's 6507 microprocessor (MPU) provides the primary decision making and computational capabilities for the drive. It is a self-contained microcomputer system on a single chip.

The MPU controls the sequence of system operations by putting addresses out to the program memory (ROM) and receiving instructions in return. It causes the system to perform the desired operation by reading an instruction (specific bit pattern) and executing that instruction. It then goes to the next instruction in the program and executes it.

The microprocessor:

- Controls data transfers through control of the common data and address buses.
- Monitors the Peripheral Interface Adaptor (PIA) for data transfers and status requests by the computer console.
- Provides control characters to notify the computer console of the status of operations performed and information received.
- Executes commands from the computer console.
- Controls the Stepper Motor Logic, Disk Drive Logic and Motor Logic, all of which are buffered in the PIA.
- Controls the 2793 Floppy Disk Controller (FDC).

The address bus, the bi-directional data bus, and the Read/Write line serve as parallel paths for data transfer in and out of the microprocessor and give it direct control over the central processing system. The address bus puts out addresses to control the source or destination of data transfers. The Read/Write line determines the direction in which data transfer occurs.

These addresses are derived from various sources within the microprocessor. During the instruction cycle from program memory (ROM), the addresses are usually derived from the program counter which controls the execution of sequential instructions. Addresses for data transfers between the microprocessor and RAM are usually derived: 1) directly from the program memory; or, 2) from the microprocessor.

## READ-ONLY MEMORY

The Disk Drive's Read-Only Memory (ROM) stores the sequence of instructions (program memory) that make up the 1050's internal control software. It contains specific operating instructions used by the microprocessor to accomplish a variety of functions. These functions include telling the 2793 Floppy Disk Controller (FDC) what task to perform.

An important characteristic of the ROM chip is that the information is stored on a permanent basis. Turning OFF the power does not cause the loss of ROM information.

## RANDOM ACCESS MEMORY (RAM)

The Disk Drive's Random Access Memory (RAM) is used by the microprocessor for temporary storage of input data, calculations and system information.

Data may be written into RAM as well as read from RAM by the microprocessor. The RAM identifies the type of data transfer by the Read/Write line. When the line is active HIGH, the operation is to Read from memory and when the line is active LOW, the operation is to Write to memory. Turning the power OFF obliterates all information in RAM.

## 6532 PERIPHERAL INTERFACE ADAPTOR (PIA)

The 6532 Peripheral Interface Adaptor (PIA) is a buffering and signal formatting device with no decision making or computational capability. It is an Input/Output (I/O) device which acts as an interface between the 6507 microprocessor, the 1050 system functions and the console.

The PIA:

- Applies the console's serial outputs to the data and address buses when requested to do so by the drive's microprocessor unit.
- Provides 128 bytes of RAM for temporary storage of status information and data sent by the Data Interface section for application to the microprocessor.
- Monitors the 2793 Floppy Disk Controller.

- o Acts as communication interface between the computer console and the microprocessor.

- o Interfaces with the Stepper Motor Logic and Drive Motor Logic.

The microprocessor communicates with the PIA through eight data lines connected to the data bus. The microprocessor initiates communication by using its address lines to select or address the PIA.

The PIA provides 16 programmable bi-directional port lines to communicate with the computer console and perform the system functions. The port lines are divided into two 8-bit ports, PAO-PA7 and PBO-PB7. PA7 may also function as an interrupt input pin. The Interrupt Request (IRQ) line is used to inform the microprocessor when a device requires servicing.

## 2793 FLOPPY DISK CONTROLLER (FDC)

The 2793 Floppy Disk Controller (FDC) and the Read/Write and Erase Logic make up the Data Interface between the disk drive's central processing system and the diskette.

The FDC is the main element of the Data Interface function. The FDC is a highly specialized microprocessor which has an arithmetic logic unit, comparator and the necessary microprogram logic to control the Read/Write operation to the diskette. It also includes an internal phase-lock loop, data separation and write precompensation logic.

The FDC:

- o Combines data, timing and data validity pulses into the serial format for recording onto diskette.

- o Separates the above signals and provides the output data in parallel during a Read operation.

- o Controls the Write and Erase logic circuitry during a Write operation.

- o Generates the data validity codes (called Cyclic Redundancy Checks or CRCs) during a Write operation and checks them during a Read operation.

- o Contains an internal phase-lock loop.

The microprocessor controls the FDC and can access any of the following registers located in the FDC: Track, Sector, Data, Command, and Status. Refer to Table 1-1 for a description of the contents of each register.

Table 1-1

FDC REGISTERS/CONTENTS

| Register | Contents |
|---|---|
| Track | Current head address. Updated automatically as the head moves across the diskette. |
| Sector | Number of the sector being considered for a Read or Write operation. |
| Data | Information read from the diskette to be transferred to the microprocessor after the necessary serial-to-parallel conversion. The FDC receives data in parallel from the microprocessor and converts the data to serial for storage on the diskette. |
| Command | Instructions from the microprocessor that are interpreted by an internally controlled programmable logic array to generate the appropriate control signals for the logical operation to be performed. |
| Status | Condition of the system. After each command is executed, the control logic issues an interrupt to the microprocessor to allow examination of the status register for any errors before resetting the interrupt. Each of the eight bits in the staus register represents a different error condition. |

The FDC controls the following elements of the Data Interface function:

- o Write/Erase Logic
- o Write Protect Logic
- o Read Logic
- o Read/Write Head
- o Erase Head

## WRITE/ERASE LOGIC

The Write/Erase Logic manages the recording of data from the Floppy Disk Controller to the diskette. It provides correct current and polarity to the Read/Write Head. (See Figure 1-7 for a block diagram of the Write/Erase Logic.) Table 1-2 describes the basic modules of the Write/Erase Logic.

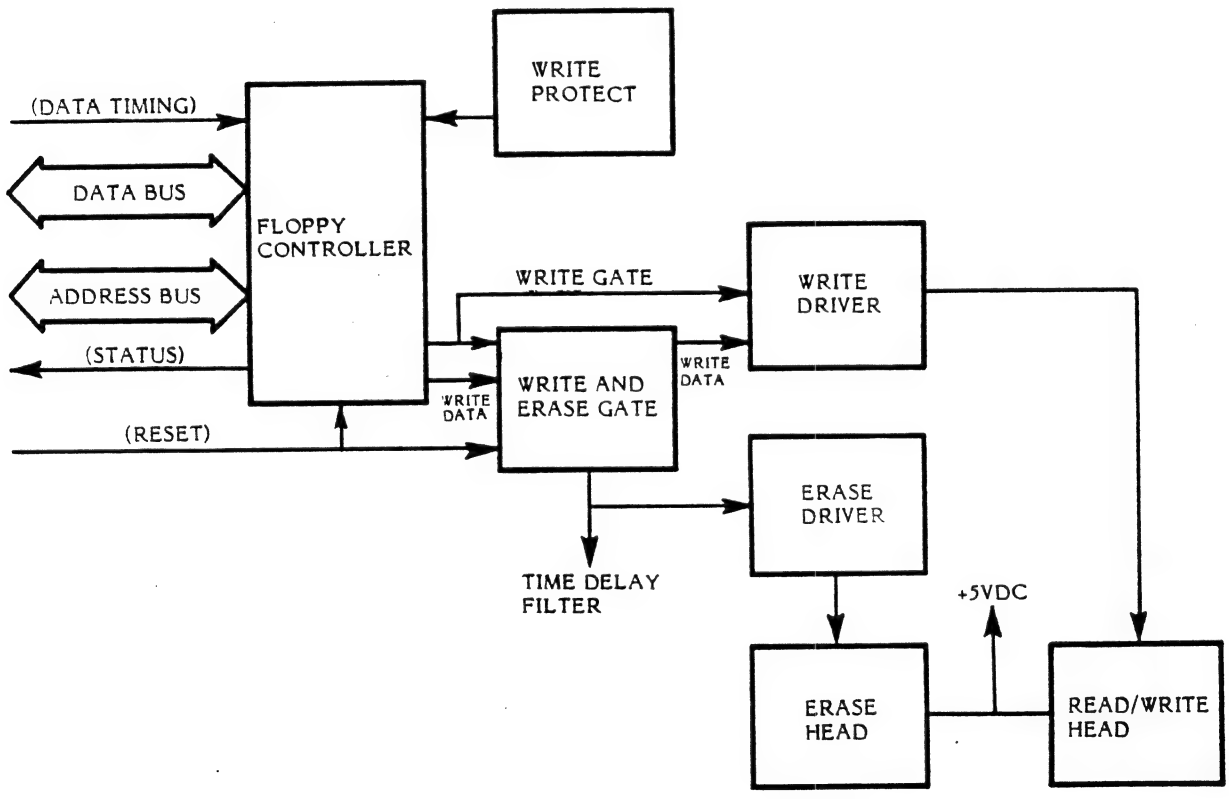



Figure 1-7. Write/Erase Logic Block Diagram

Table 1-2

WRITE/ERASE LOGIC

| Element | Function |
|---|---|
| Write Driver | Enables Write function and limits the Write currents. |
| Write and Erase Gate | Turns on both the Write and Erase Drivers during a Write operation and turns them off during a Read operation |
| Erase Driver | Drives the Erase Head during a Write operation. |

## WRITE-PROTECT LOGIC

The Write-Protect Logic prevents writing to a diskette by informing the Floppy Disk Controller when a write-protected diskette is inserted in the drive. Each diskette contains a notched area in the upper right hand corner which allows light from the LED to hit the base of the phototransistor. On a write-protected diskette the light is blocked by a tab or opaque material on the diskette. This turns off the phototransistor and the output from U11 is clamped Low. The low input to the FDC signals that a write-protected diskette is inserted and you cannot write to it.

## READ LOGIC

The Read Logic is used to retrieve data from the diskette and input the data into the FDC. It shapes pulses into the correct format to be read by the FDC. (See Figure 1-8 for a block diagram of the Read Logic.) Table 1-3 describes the Read Logic functions.

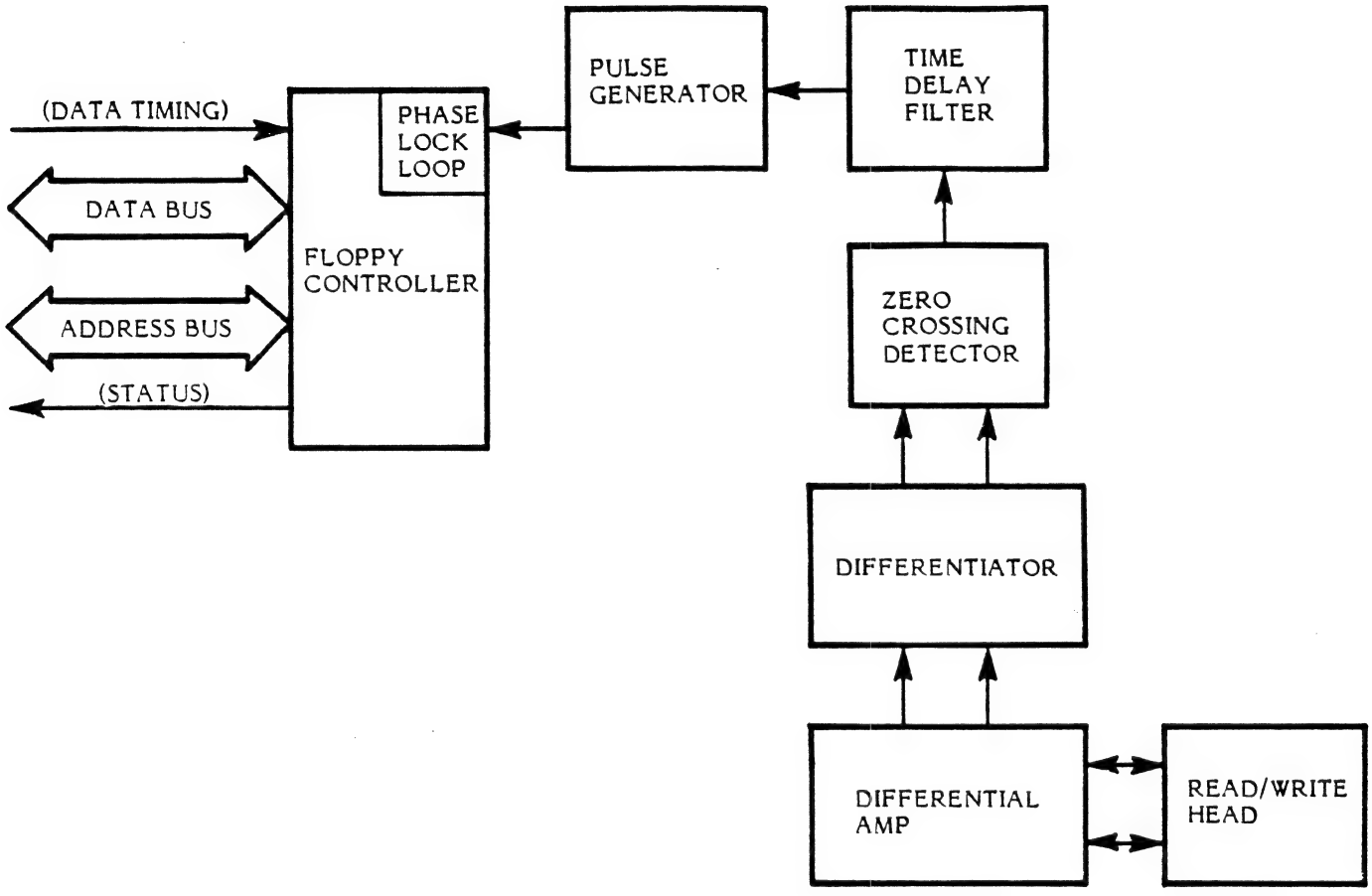



Figure 1-8. Read Logic Block Diagram

Table 1-3

READ LOGIC ELEMENTS

| Element | Function |
|---|---|
| Differential Amp | Initial amplification of Read/ Write head signals. |
| Differentiator | Squaring up the two differential amp outputs. |
| Zero Crossing Detector | The single output changes level whenever the two 180 degrees out-of-phase input signals cross their zero axis coincidentally. This eliminates false pulses caused by Read/Write Head signal decay, rather than intentional signal level changes. |
| Time Delay Filter | Digital Filter |
| Pulse Generator | Produces a single pulse out for each logic level transition at its output. This results in the reproduction of the original FDC signal. |

## READ/WRITE HEAD

The Read/Write Head is an electro-magnetic device used for interfacing with the magnetic recording media. It converts magnetic flux changes to electric current, and vice versa, through the use of a center tapped coil.

Current is passed through the windings on the head core. Data is written to the diskette surface by changing the direction of the current through the Read/Write Head (each flux change equals a data bit.)

Data is read from the diskette when signals from the head coil windings are applied to the differential amplifier.

## ERASE HEAD

The Erase Head creates a guardband (a blank space between tracks) in order to prevent one recorded track from interfering with either the next inner or next outer track.

It straddles the Read/Write Head in such a way that after the data is written onto the diskette, the Erase Head "tunnel" narrows the track width, leaving guardbands between tracks (See Figure 1-9).

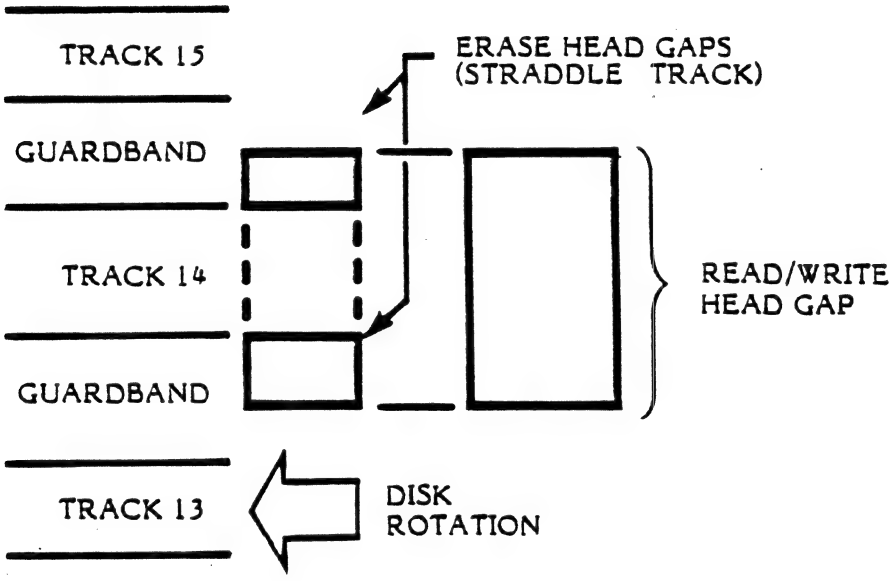



Figure 1-9. Erase Head Gaps

## SERIAL BUS LINE ASSIGNMENTS

The computer communicates with peripheral devices via a serial port which consists of a serial DATA OUT (transmission) line, a serial DATA IN (receiver) line and miscellaneous control lines.

Data is transmitted and received as 8 bits of serial data (least significant bit sent first) preceded by a logic zero start bit and succeeded by a logic one stop bit. The serial DATA OUT is transmitted as a positive logic (+4v = one/true/HIGH, Ov = zero/false/LOW). The serial DATA OUT line always assumes its new state when the serial CLOCK OUT line goes HIGH; CLOCK OUT then goes LOW in the center of the DATA OUT bit time.

Table 1-5 describes the function of the serial bus connector pins.

Table 1-4

Serial Bus Line Assignments

| Pin No. | Description |
|---|---|
| 1 | CLOCK IN is not used by the current DOS and peripherals. This line is reserved for future synchronous communications. |
| 2 | CLOCK OUT is the serial bus clock. CLOCK OUT goes HIGH at the start of each DATA OUT bit and returns to LOW in the middle of each bit. |
| 3 | DATA IN is the serial bus data line to the computer. |
| 4 | GND is the signal/shield ground line. |
| 5 | DATA OUT is the serial bus data line from the computer. |
| 6 | GND is the signal/shield ground line. |
| 7 | COMMAND is normally HIGH and goes LOW when a command frame is being sent from the computer. |
| 8 | MOTOR CONTROL is the cassette motor control line (HIGH=on, LOW=off). |
| 9 | PROCEED is not used by the current DOS and peripherals. This line is pulled HIGH passively inside the computer. |
| 10 | +5v/READY indicates that the computer is turned on and ready. This line may also be used as a +5 volt supply of 50 uA current rating, for Atari peripherals only. |
| 11 | AUDIO IN accepts an audio signal from the diskette. |
| 12 | +12v supply for Atari peripherals only. |
| 13 | INTERRUPT is not used by the current DOS or peripherals. This line is pulled HIGH passively inside the computer. |

There are no pin reassignments made in the serial bus cable, so pin 3, the computer's DATA IN line, is also the peripheral's data output line the same holds true for pin 5.

## SERIAL BUS ELECTRICAL SPECIFICATIONS

Peripheral Input:
VIH = 2.0v minimum
VIL = 0.4v maximum

IIH = 20uA maximum at VIH = 2.0v
IIL = 5uA maximum at VIL = 0.4v

Peripheral Output (open collector bipolar):
VOH = 4.5v minimum with external 100K ohm pull-up
VOL = 0.4v maximum at 1.6 uA

Vcc/READY Input:
VIH = 2.0v minimum at IIH = 1uA maximum
VIL = 0.4v maximum
Input goes to logic zero when open

## SERIAL BUS PROTOCOL

When a command line goes LOW, the computer console sends a command frame to all devices. The command provides the disk drive with the following information:

- Serial Bus Device ID
- Command
- Two bytes of auxiliary information
- Checksum

The commands supported by the disk controller are: Get Sector, Put Sector, Put Sector with Verify, Status Request, and Format Disk.

# SECTION 2

# 1050 DISK DRIVE

# TEST EQUIPMENT/DIAGNOSTIC TESTS

Equipment Requirements:

- o 400 Computer with 16K of RAM
- o Television
- o Oscilloscope at least 15MHz
- o Digital Voltmeter
- o ATARI 1050 Disk Drive Diagnostic Diskette ( FD100690)
- o Dymek Alignment Diskette (TE017575)
- o Work Diskette (FD100053)
- o Preformatted Diskette (FD100026)
- o Assorted Small Tools
- o Printer (Optional)

Hook-Up:

- o Set up the disk drive and computer according to the procedures in the 1050 Owner's Guide.

- o Set the drive select switches to the Drive 1 position.

- o Be certain all connections are secure.

Check Of Mechanical Components:

Before testing the Disk Drive, be certain of the following:

- o Check that the diskette enable lever moves freely and locks in the perpendicular position.

- o Insert a diskette in the slot and push it all the way in. Make sure that the eject mechanism clicks into position. Now move the diskette enable lever around to the perpendicular position to lock. Make sure that the diskette is ejected when the diskette enable lever is returned to the parallel position.

Diagnostic Tests:

The tests in this section are intended to assist you in diagnosing possible problems in the 1050 Disk Drive. All diagnostic and functional tests are reviewed in this section. Use these tests in conjunction with the symptom checklists, waveform diagrams, and schematics to troubleshoot the unit under test.

## Power-Up Test

Purpose: To test the disk drive's electronic hardware Initialization and Reset. This test prepares the drive for further testing. The drive must pass this test before other tests can be performed.

Special Tools Required: None

Procedure:

1. Connect disk drive to computer (Page 1-3).
2. Turn the disk drive power switch ON.
3. Observe that the following occur.
   a. The Power LED lights.
   b. The Activity LED lights.
   c. The Drive Motor turns on.
   d. The Head Carriage steps to track 0 (outer track).
   e. Several seconds pass, and the Drive Motor and the Activity LED turn off.
4. This completes the Power-up Test.

This test indicates that the unit passed all of its internal diagnostics. The internal diagnostic test checks the following six elements.

A. Input/Output Device

The 6532 device is initialized and verified. Upon incorrect comparison, the processor will flag ERROR.

B. Disk Controller Device

The 2793 device is tested for access to the track, and sector registers, followed by an internal functional test. Upon error, the processor will flag ERROR.

C. ROM Checksum

The processor verifies PROM validity by performing a checksum on it. Upon error, the processor will flag ERROR and discontinue testing.

D. RAM Check

Unique values are written to each RAM location, and then each location is read to verify it contains the correct value. Upon error, the processor will flag ERROR and discontinue testing.

E. Error Flag Stop

Upon any ERROR flag being set, the processor will discontinue testing and place the unit in a hard failure state (2-second cycle off/on of spindle motor).

F. Restore Check

Track 0 is sought by stepping the head away from spindle until track 0 sensor is detected and motor phase is 1. Upon stepping more than 50 tracks without finding the track 0 sensor, the unit will fail and enter the hard failure state.

Loading The Diagnostic Test Diskette:

Insert the Diagnostic Diskette and turn the diskette enable lever down. The activity LED lights, and the motor spins for about five seconds, centering the diskette on the spindle.

Now Power-Up the computer without a cartridge installed. The Diagnostic Test will boot-up and display the two main menu options on the TV screen.

These two options are:

1. Run Diagnostic Tests
2. Troubleshooting Options

Make selection 1 and hit the RETURN key. The diagnostic testing will run automatically. These pass or fail tests, will indicate which section of the disk drive to start your troubleshooting in. The following is a detailed description of each test.

| | | |
|---|---|---|
| Controller Test | - | This checks that the FDC2793 floppy disk controller chip will recognize a command or data frame from the computer. A failure here indicates a defective FDC2793 IC. |
| Invalid Command Test | - | This checks that the FDC2793 floppy disk controller chip will recognize an illegal command or data frame and not try to execute on it. |
| Write Protect Test | - | This checks out the Write Protect Sensor and related circuitry. |
| NOTE | - | If Write Protect is constantly on check to be sure that dirt has not blocked the hole where the lower part of the sensor is located. |

| | | |
|---|---|---|
| Motor Start Test | - | This test checks the elapsed time between starting the spindle motor from a dead start to the point where valid data is read from the diskette. If this test fails a motor control circuit or a read circuit failure is indicated. |
| Motor Speed Test | - | This test checks the speed of the spindle motor in milliseconds. If the speed is too low or too high use the speed calibration option in the troubleshooting section of the Diagnostic Program Disk to adjust (VR2) with a screwdriver. |
| Head Step & Settle Test | - | This test checks the capability of the drive to read a sector, step to the next track, and read another sector within a specified amount of time. A failure here would indicate a bad drive mechanism, or a defect in the read circuitry. |
| Track 00 Test | - | This test steps the R/W Head out to track 02 then steps back to track 00 and checks the status of the track 00 sensor. |

If this test fails use the track zero sensor calibration option in the troubleshooting section of this diagnostic program to adjust the sensor.

At the end of the Diagnostic Tests, you are again given the choice of:

1. Run Diagnostic Tests
2. Troubleshooting Options

Select 2 and hit RETURN. This will give you the troubleshooting options menu.

This section combined with the symptom checklists, circuit waveforms, and schematics, will help you to troubleshoot or make adjustment to various circuits in the 1050 disk drive.

Read the instructions and follow the prompts, displayed on the screen, carefully.

NOTE: If the unit under test "Hangs" (eg...no response to an abort command by the computer), turn off the 1050 disk drive, remove the diskette, turn the 1050 back on, insert the diskette back in, and redo the test.

The following is a detailed description of the troubleshooting options:

**1. Loop on Speed Calibration**

Use this option to set the spindle speed. Adjust VR2 for a speed of 208.3 milliseconds +/- 1.0 millisecond

**2. Run Manual Alignment Tests**

The following four tests are designed to check out the drive mechanism alignment. Use the Dymek Analog Alignment Diskette (Part #TEO17575).

Set up the oscilloscope as follows:

| | |
|---|---|
| Channel A | Normal |
| Channel B | Inverted |
| Vertical Mode | Add, Ch. A & B |
| Time/Div | 2uS/Div |
| Volts/Div | 20MV/Div (X10 Probes) |
| | AC (Ch. A & B) |
| Trigger | Internal (Ch A), AC, Normal, |
| | Positive slope |

Set up the probes as follows:

| | |
|---|---|
| Channel A | TP 3 on PCBA |
| Channel B | TP 4 on PCBA |
| Ground | TP 17 on PCBA |

Use track 0 to double check the spindle speed of the drive mechanism on track 00. The time for one cycle of the sinewave is approx. 16.6uS

Use track 16 to check or adjust the radial track alignment.

(Cats-Eyes). Set the time/div at 20ms/Div and follow the instructions below.

Verify that cats-eye lobes are present on the oscilloscope and observe the lobe ratio of the cats-eyes. The lobe ratio is the amplitude of the smaller lobe divided by the amplitude of the larger lobe. The ideal lobe ratio is 100% (both lobes equal). Refer to Figure 2-1 for examples.

Align the TM50-1 drive by loosening the screws on the stepper motor (see Figure 2-2) and then rotate the motor until the lobe ratio is 100%. Recheck the track 0 sensor adjustment, then recheck lobe ratio. Repeat until the alignment is within 80-100%. Tighten down stepper motor screws.

Use trk 33 to check the head load pad pressure. Set the time/div to 0.5ms/div, and set the volts/div to 50mv/div.

There should be a broadband display on the oscilloscope. With your index finger press very lightly on the top of the pressure pad (See Figure 2-2). If the amplitude increases greatly (more than 20%) then use a flat blade screwdriver to turn the pressure pad 1/4 of a turn at a time. After 3/4 of a turn assume the pressure pad to be bad and replace it.

Use trk 34 to check the Head Azimuth. Set the time/div for 0.5ms/div, and set the volts/div for 50mv/div.

See Figure 2-3 for the correct waveforms.

Note: If the Azimuth is greater than + or - 18 min. of angle, replace the drive mechanism.

Use the ESC key to stop the test, and the RETURN key to return to the menu.

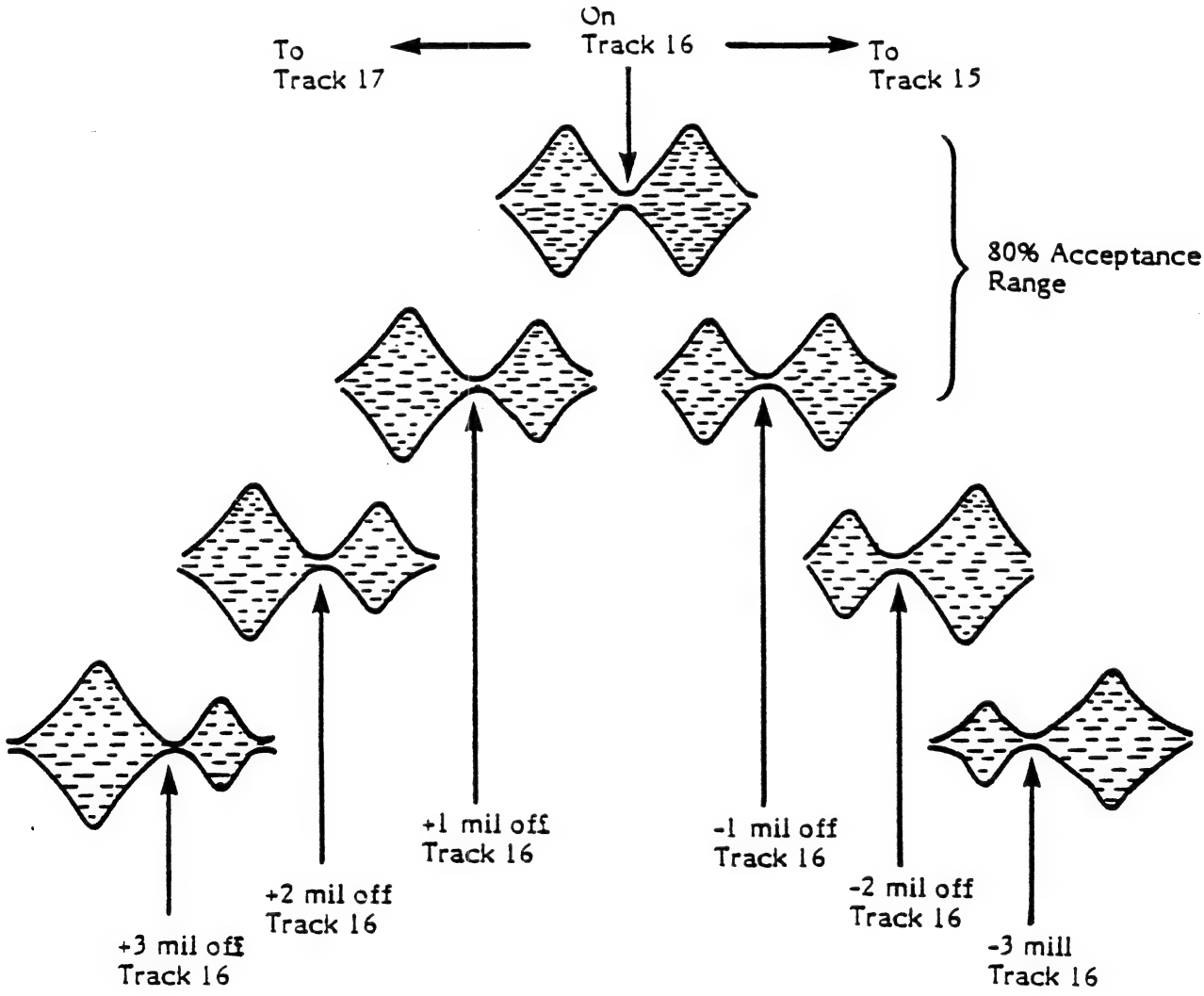



Figure 2-1. Amplitude Variation of Cat's Eye

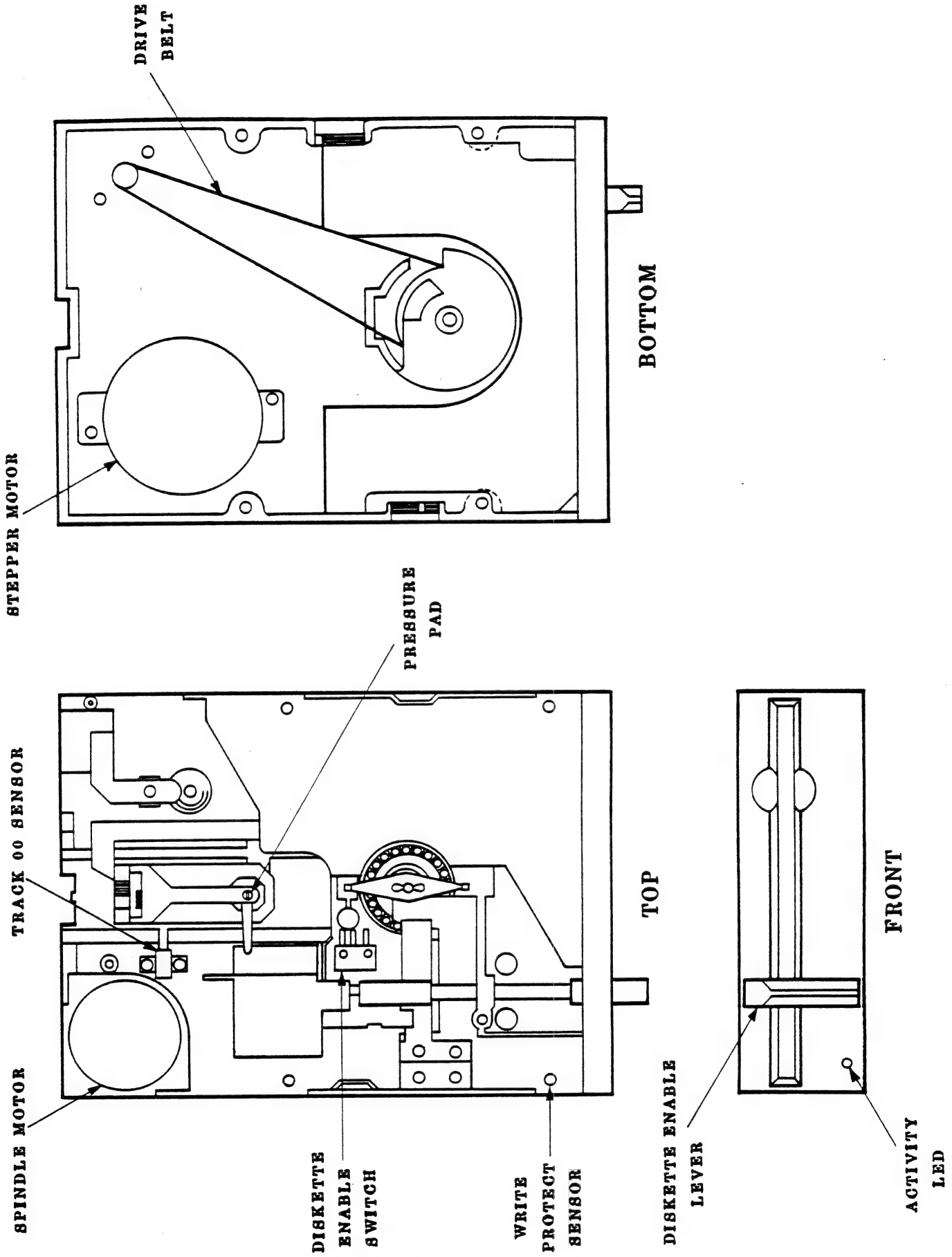



Figure 2-2. Adjustment Points.

NOTE

Atari recommends replacement of the entire Drive Mechanism if the Azimuth is out of the specified range, due to the complexity of the adjustment. For this reason, be certain that the Azimuth is out of specification before replacement.

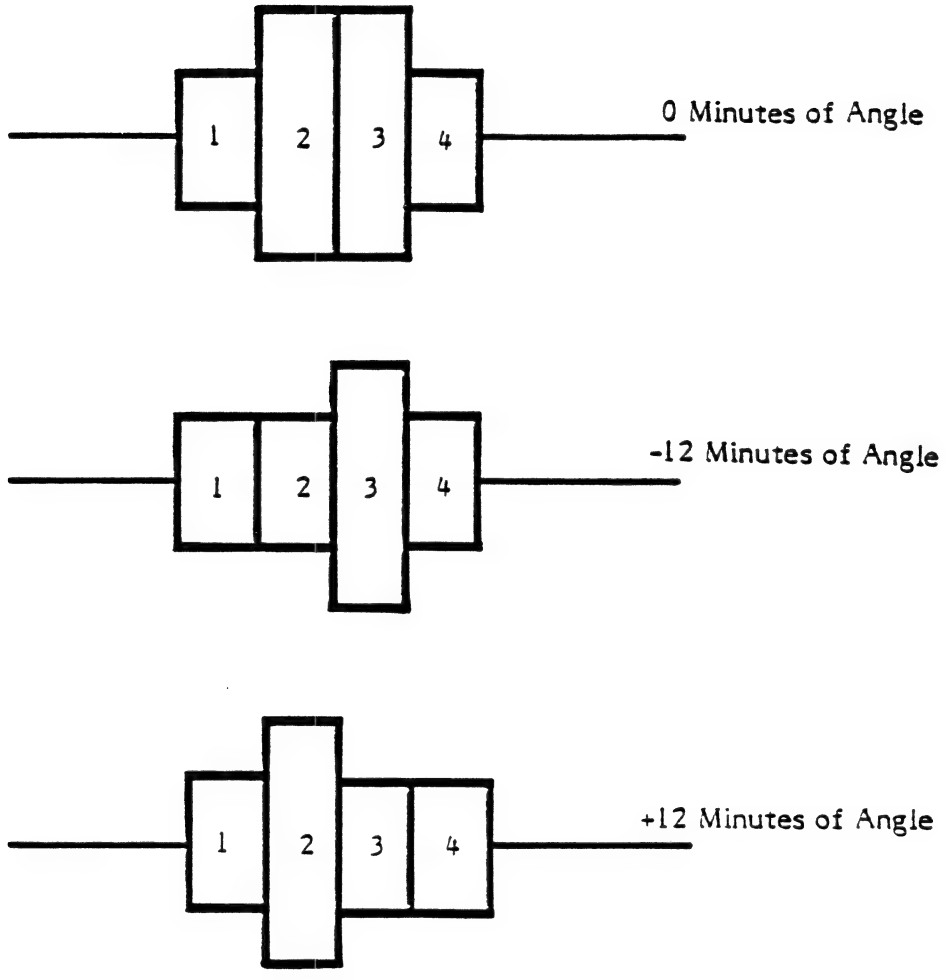



Figure 2-3. Head Azimuth Waveform

3. **Drive Select Switch Test**

   This test is to assure that the disk drive can be selected in all four positions. Check all four positions, then return to drive #1 position. There is a slight delay and then an automatic return to menu when this test is done.

Note: If this test fails in any position, then check out the switch first, and PIA chip second.

4. **Single Density Burn-In (10 min)**

   This is a short test to check for compatability between drives. A failure on this test indicates an alignment problem. (See Option 2 on troubleshooting options.)

This test first does a write to all sectors (E5 pattern), then it does a read of all sectors. Be sure to use preformatted diskette # FD100026.

### 5. Double Density Burn-In (2 Hours)

This test formats the diskette in double density, writes and reads all data fields with a sequential seek, and writes and reads all data fields with an accordian seek.

Errors are logged into the first and third sector on the track where they occur. These errors can be printed out on the printer using the printout option in the troubleshooting options of the diagnostic test program.

Note: Once this test has been started, the 1050 should be disconnected from the SIO line the testing will continue until the pass counter reaches zero. This test will abort if:

1. The drive fails to format or verify format.
2. The drive fails to read or write the error logs (sectors 1 or 3 on each track).
3. More than 128 errors occur in any one sector.

### 6. Error Printout

This option is used in conjunction with the double density burn-in described above to printout the error logs written on each track.

Figure 2-4 contains two examples of this printout and how to interpret them.

```
1050 BURN-IN (2HR), REV.A


SERIAL I.D. = 3456789012

PASS COUNTER = 0
PASS COUNT RECEIVED = 24

TRACK 31 - ERRORS
  SECTOR 16   ERROR STATUS = $01
  DATA BYTE LOCATION = 47

  DATA  DATA  DATA  DATA  SEEK  RNF
  CRC   LOST  HARD  SOFT
  0     0     0     1     0     0

TRACK 31 - ERRORS
  SECTOR 20   ERROR STATUS = $02

  DATA  DATA  DATA  DATA  SEEK  RNF
  CRC   LOST  HARD  SOFT
  1     0     0     0     0     0

TRACK 33 - ERRORS
  SECTOR 4    ERROR STATUS = $01
  DATA BYTE LOCATION = 77

  DATA  DATA  DATA  DATA  SEEK  RNF
  CRC   LOST  HARD  SOFT
  0     0     0     1     0     0
```

**EXAMPLE 1**

```
1050 BURN-IN (2HR), REV.A


SERIAL I.D. = 1234FG7890

PASS COUNTER = 24
PASS COUNT RECEIVED = 24

NO ERRORS-ALL TRACKS
```

**EXAMPLE 2**

Figure 2-4. Error Log Printout

Example 1 - Is an example of the error logs which are recorded during the double density burn-in routine.

Example 2 - Is an example of the printout from a perfect burn-in test.

The use of this error printout is quite subjective. You may have several errors and still have a good drive. We will attempt to give you a feel for what the major concerns are.

The first thing to look at is the pass counter this should equal the number in the pass count received. This indicates that the drive performed burn-in with no major failures.

The next thing to look for is many errors of the same type located on the same track and/or sector. If this occurs, run the burn-in test again using a different blank diskette if the problem still exists then there is probably a hardware failure.

The next thing to look for is the type of errors most commonly found. Below are some clues as to the cause of the error types:

Data CRC - If several of these errors occur replace the WD2793 controller IC. Troubleshoot the read and write circuits.

Data Lost - This indicates a problem in transferring data between the WD2793 and the 6810 RAM IC.

Data Hard - This occurs when data cannot be found after many retrys. Check the write circuit, and diskette for flaws.

Data Soft - This indicates that data was not read on the first pass, but in subsequent passes was found. If many of these occur in several different locations suspect the speed adjustment or WD2793.

Seek - Many seek errors would indicate a bad diskette, or an alignment problem (cats-eyes).

RNF - Many RNF errors in the same location would indicate bad diskette. Many RNF errors in different locations indicates a bad WD2793 controller.

**7. Track Zero Sensor Calibration**

This option is used to check and adjust the track zero sensor.

If the sensor is misadjusted the screen will display either "forward", "backward", indicating which direction the sensor needs to be moved. To adjust the sensor, (See Figure 2-2) loosen the screw holding it in place and move the sensor backward or forward as dictated by the screen, until the screen displays "sensor OK".

Note: Be careful! This is a slight adjustment which doesn't take much movement to correct. Hold the sensor in position while tightening down the screw.

## SECTION 3

## DISASSEMBLY/ASSEMBLY OF THE 1050 DISK DRIVE

Turn the unit over; remove the four screws from the bottom cover and the two screws holding the lower part of the front bezel, as illustrated in Figure 3-2.

Holding the top and bottom covers together, turn the unit right side up.

Carefully pull the lower part of the front bezel forward and at the same time lift off the top cover. (Be careful not to break the thin plastic tabs attaching the top of the front bezel to the top cover.)

The drive mechanism rests on four dowels above the PCB. To remove it, disconnect the plugs from the PCB and lift it out. Be sure to attach them according to Figure 3-1 below.

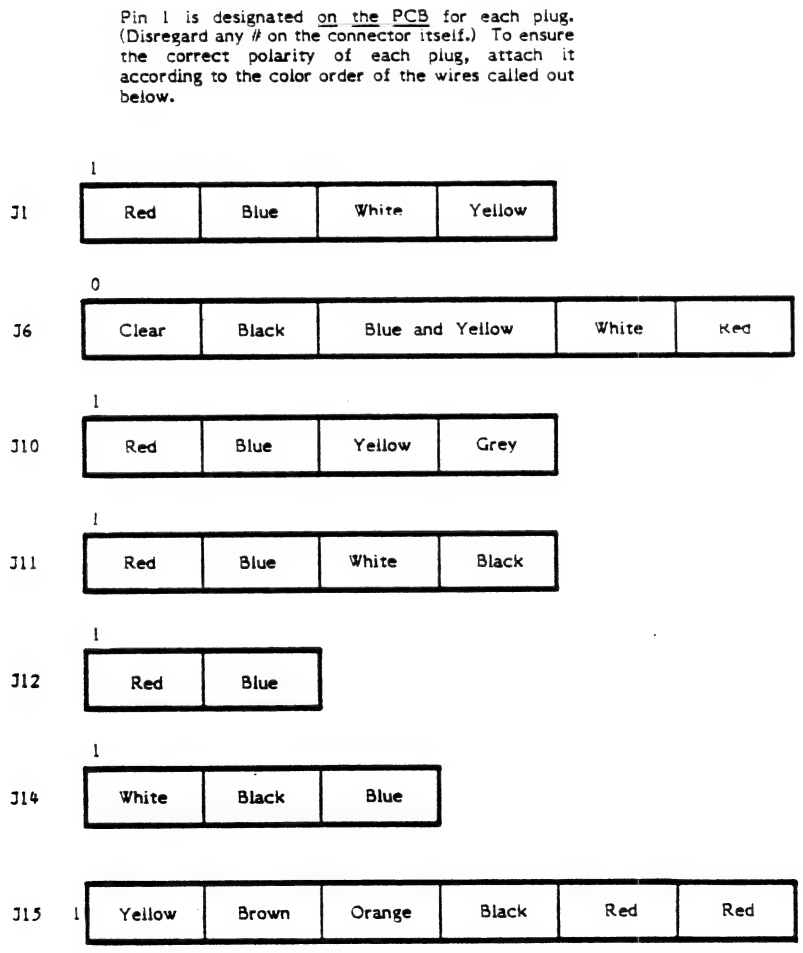



Figure 3-1. Polarity of Drive Mechanism Plugs

The PC board snaps into the bottom of the lower cover and fits over the three alignment guides located in it.

The upper and lower RF shields are attached to the PCB by four bend tabs. When removing the top shield, be sure to note where the cutouts are located and replace it the same way.

The five LSI's are located under the shield. No adjustment to the variable capacitor or resistors is needed when replacing the 2793FDC chip.

Reassemble in the reverse order.

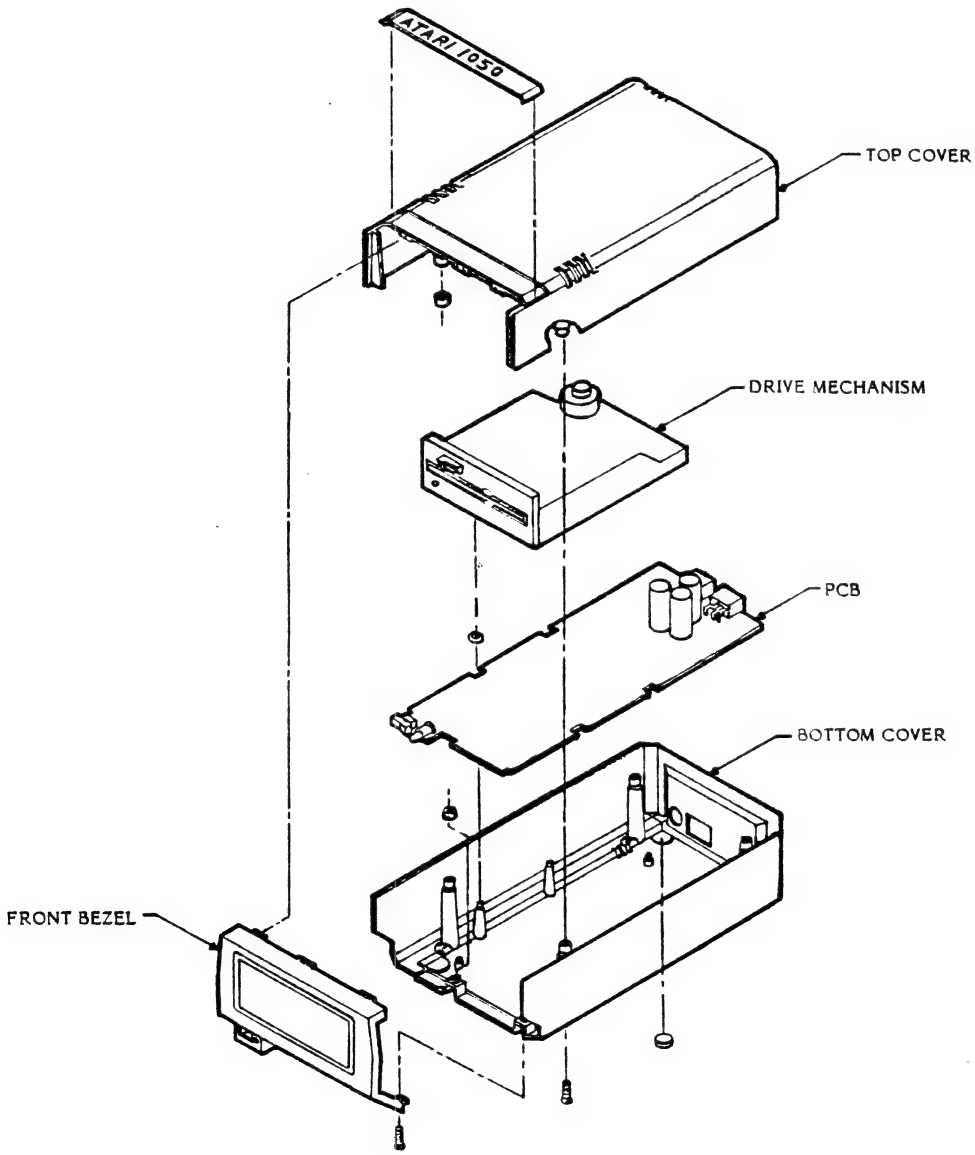



Figure 3-2. 1050 Disassembly

## SECTION 4

## SYMPTOM CHECKLIST

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| **DRIVE MOTOR AND SPEED PROBLEMS** | | |
| Drive motor doesn't rotate when latch is shut (no activity LED) | Defective diskette enable switch | Replace Diskette Enable switch assembly on drive mechanism. |
| | Intermittent or bad connection | Check that P1 is properly connected to J1 |
| | Defective Diskette Enable circuit (U6) | Troubleshoot and replace defective component (See waveforms, p. 4-11) |
| | Defective component in motor control circuit (Q4, Q6, U5, VR2) | Troubleshoot and replace defective component (see waveforms, p. 4-8) |
| | Defective drive motor | Replace drive motor |
| Drive motor operates sporadically | Intermittent or bad connection | Check that P1 is properly connected to J1 |
| | Defective component in motor control circuit (U5, VR2, Q4, Q6) | Troubleshoot and replace defective component (see waveforms, p. 4-8) |
| | Defective component in tachometer feedback circuit (U5, VR2, Q6) | Troubleshoot and replace defective component (see waveforms, p. 4-9) |
| | Open winding in drive motor tachometer | Replace drive motor |
| Drive motor speed too slow or too fast | Speed adjustment incorrect | Adjust speed POT (VR2) for speed of 208.3 ms |
| Speed not adjustable | Defective component in tachometer feedback circuit (VR2, U5, Q6) | Troubleshoot and replace defective component (see waveforms, p. 4-9) |
| | Open winding in drive motor tachometer | Replace drive motor |

## SYMPTOM CHECKLIST (Continued)

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| **DRIVE MOTOR AND SPEED PROBLEMS** (Continued) | | |
| Drive motor speed unstable | Intermittent or bad connection | Check that P1 is properly connected to J1 (refer to Figure 3-1). |
| | Drive belt slipping | Replace drive mechanism |
| | Improper cone pressure on diskette | Replace drive mechanism |
| | Defective component in tach feedback circuit (U5, Q6, VR2) | Troubleshoot and replace defective component (see waveforms, p. 4-9) |
| | Drive motor bearings | Replace drive motor |
| **STEPPER MOTOR PROBLEMS** | | |
| Head positioner will not step | Bad connection at J15 | Check for proper connection and polarity at J15 (refer to Figure 3-1). |
| | Defective component in stepper driver circuit (U2, U3, U7) | Troubleshoot and replace defective component (see waveforms, p. 4-10) |
| | Defective stepper motor | Replace drive mechanism |
| Skips or missteps to wrong tracks | Bad connection at J15 | Check for proper connection and polarity at J15 (refer to Figure 3-1). |
| | Defective component in stepper driver circuit (U2, U3, U7) | Troubleshoot and replace defective component (see waveforms, p. 4-10) |
| | Band pully or head carriage binding | Replace drive mechanism |
| | Track 00 sensor defective needs adjustment Q5 | Troubleshoot and replace or adjust defective component (see waveforms, p. 4-11) |
| **DRIVE MECHANISM PROBLEMS** | | |
| Diskette will not eject | Eject assembly binding or broken | Replace drive mechanism |

## SYMPTOM CHECKLIST (Continued)

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| **DRIVE MECHANISM PROBLEMS** (Continued) | | |
| Drive will not pass track 00 sensor test | Track 00 sensor defective or needs adjustment | Troubleshoot and replace or adjust defective component |
| | Carriage stop missing or improperly set | Replace drive mechanism |
| | Defective component in track 00 sensor circuit (Q5, U13) | Troubleshoot and replace defective component (see waveforms, p. 4-11) |
| Intermittent Read/Write errors | Head load pad pressure | Replace drive mechanism |
| | Dirty Read/Write head | Clean head with 91% Isopropyl Alcohol |
| | Burned head | Replace drive mechanism |
| Diskette incompatibility | Radial track alignment | Adjust "Cats Eyes" alignment |
| | Head Azimuth alignment | Check head azimuth. If out of spec., replace drive mechanism. |
| | Drive belt slipping | Replace drive mechanism |
| | Speed improperly adjusted (VR2) | Check and adjust for proper speed on both drives |
| **READ PROBLEMS** | | |
| Soft Read errors (intermittent or non-permanent) | Defective Diskette | Try diskette on known-good drive |
| | Dirty Read/Write head | Clean head with 91% Isopropyl Alcohol |
| | Drive belt slipping | Replace drive mechanism |
| | Excessive noise in Read signal (U13, U18-20, U22-24) | Troubleshoot Read circuit (see waveforms, p. 4-12) |

## SYMPTOM CHECKLIST (Continued)

### READ PROBLEMS (Continued)

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| | Intermittent or marginal component in Read circuit (U13, U18-20, U22-24) | Troubleshoot and replace defective component (see waveforms, p. 4-12) |
| Fails to Read anything | Improper connection of J6 | Check for correct polarity (refer to Figure 3-1). |
| | Failed component in read circuit (U13, U18-20, U22-24). | Troubleshoot and replace failed component (see waveforms, p. 4-12) |
| | Burned Head | Replace drive mechanism |
| | Speed adjustment incorrect | Adjust speed POT (VR2) to speed of 208.3ms |
| | Head load pad pressure | Replace drive mechanism |
| | Dirty Read/Write head | Clean head with 91% Isopropyl alcohol |
| | Burned head | Replace drive mechanism |
| | Radial track alignment | Adjust "Cats Eyes" alignment |
| | Head azimuth alignment | Check head azimuth. If out of spec., replace drive mechanism. |

### WRITE PROBLEMS

| | | |
|---|---|---|
| Fails to Write anything | Improper connection of J6 | Check for correct polarity (refer to Figure 3-1) |
| | Dirty Read/Write head | Clean head with 91% Isopropyl Alcohol |
| | Defective Write protect circuit (U11, U13) | Troubleshoot and replace defective component (see waveforms, p. 4-13) |
| | Component failure in Write circuit (U13, U15-18, U21, Q1) | Troubleshoot and replace defective component (see waveforms, p. 4-14) |
| | Defective component in Erase circuit (U11, U15 U17) | Troubleshoot and replace defective component (see waveforms, p. 4-15) |

## SYMPTOM CHECKLIST (Continued)

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| | **WRITE PROBLEMS** (Continued) | |
| | Burned head | Replace drive mechanism |
| Error 144 during Write or format routine | Defective Write protect circuit (U11, U13) | Troubleshoot and replace defective component (See waveforms p. 4-13) |
| Writes garbled data | Defective component in Erase circuit (U11,U15 U17) | Troubleshoot and replace defective component (See waveforms p. 4-15) |
| | Component failure in Write circuit (U13, U15-18, U21, Q1) | Troubleshoot and replace defective component (see waveforms, p. 4-14) |
| | Dirty Read/Write head | Clean head with 91% Isopropyl Alcohol |
| Drive is always or never Write protected | Defective Write protect circuit (U11, U13) | Troubleshoot and replace defective component (see waveforms, p. 4-13) |
| | Defective Write protect photo sensor | Replace drive mechanism |
| | **POWER SUPPLY PROBLEMS** | |
| No power or blows power | Defective bridge diodes | Replace all four diodes (CR17-CR20) (see waveforms, p. 4-16) |
| | Defective power adaptor | Replace power adaptor |
| No +5 volts at TP13 | Defective 5V regulator | Replace Q7 |
| Power LED not lit | Defective 5V regulator | Replce Q7 |
| | Defective LED | Replace CR21 |
| No +12 Volts at TP14 | Defective 12V regulator | Replace Q8 |
| | 12 volt doubler circuit | Replace CR15 & CR16, or C71 (see waveforms, p. 4-16) |

## SYMPTOM CHECKLIST (Continued)

| SYMPTOM | POSSIBLE CAUSE | CORRECTIVE ACTION |
|---|---|---|
| | **DATA INTERFACE PROBLEMS** | |
| No response to commands from computer | I/O cable or connections | Replace cable or tighten connections |
| | Command signal not getting to PIA (U7) | Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17) |
| | Defective PIA | Replace U7 |
| No data output from drive to computer | I/O cable or connections | Replace cable or tighten connections |
| | Data signal from PIA not getting to I/O connection | Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17) |
| | Defective PIA | Replace U7 |
| No data input from computer to drive | I/O cable or connections | Replace cable or tighten connections |
| | Data signal not getting to PIA (U7) | Trace signal through (U1) and replace, if necessary (see waveforms, p. 4-17) |
| No data input from computer to drive (continued) | Defective PIA | Replace U7 |
| Drive doesn't reboot when computer is powered down and then up again | VCC Ready signal not getting to PIA | Trace signal through (U1) and replace, if necessary (see waveforms, p. 4-17) |
| | Defective PIA | Replace U7 |
| | **DRIVE SELECT PROBLEMS** | |
| Drive select test fails | Defective select switch | Replace S2 |
| | Defective PIA | Replace U7 |

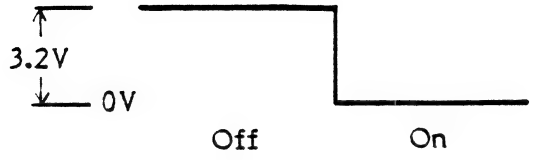
## CENTRAL PROCESSING UNIT PROBLEMS

If the other circuits have been checked and found good, one of the IC's in the CPU circuit is defective.

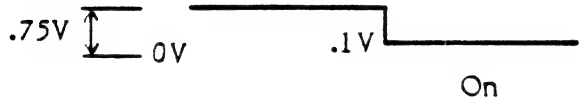
| TYPE OF FAILURE | POSSIBLE CAUSES |
|---|---|
| Power-Up failures | PIA (U7) |
| Boot Errors | 2793, FDC (U13) |
| Stepper motor failures | Microprocessor, 6507 (U9) |
| Drive motor failures | Custom ROM (U10) |
| I/O failures | RAM, 6810 (U8) |
| Drive code switch not recognized | 74LS04, Inverter (U16) |
| | 4 MHz Crystal (Y1) |
| | 74LS74,D-type, edge-triggered, flip-flop (U1) |
| | 555 Timer (U4) |
| | 74LS00, Nand gate (U6), (U12) |

NOTE: There is no relationship between the order of failures and possible causes.

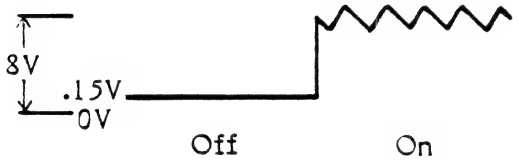
## MOTOR CONTROL SIGNALS



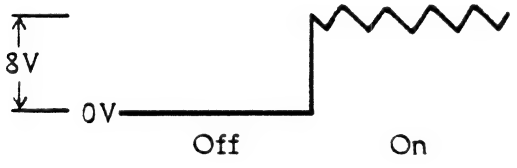

Pin 11 of U7
Schematics, Pg. 5-5



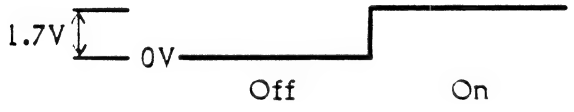

Base of Q4
Schematics, Pg. 5-7




Collector of Q4
Schematics, Pg. 5-7



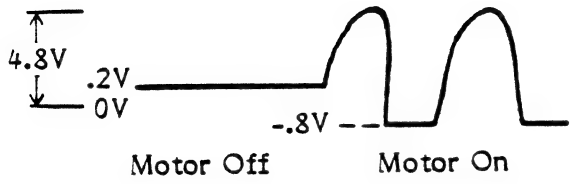

Emitter of Q6
Schematics, Pg. 5-7



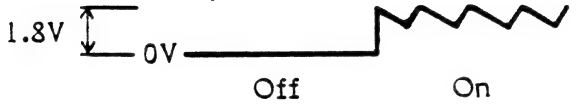

Pin 1 of J12
Schematics, Pg. 5-7

The collector of Q6 is a constant 12 volts.

## TACH FEED BACK SIGNALS/SPEED ADJUST




Pin 11 of U5
Schematics, Pg. 5-7

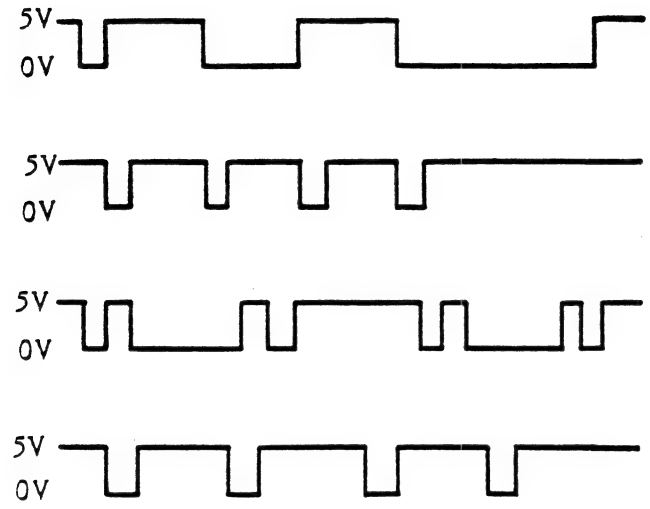



Pin 5 of U5
Schematics, Pg. 5-7

Pin 9 of U5 is a Constant 8 volts.

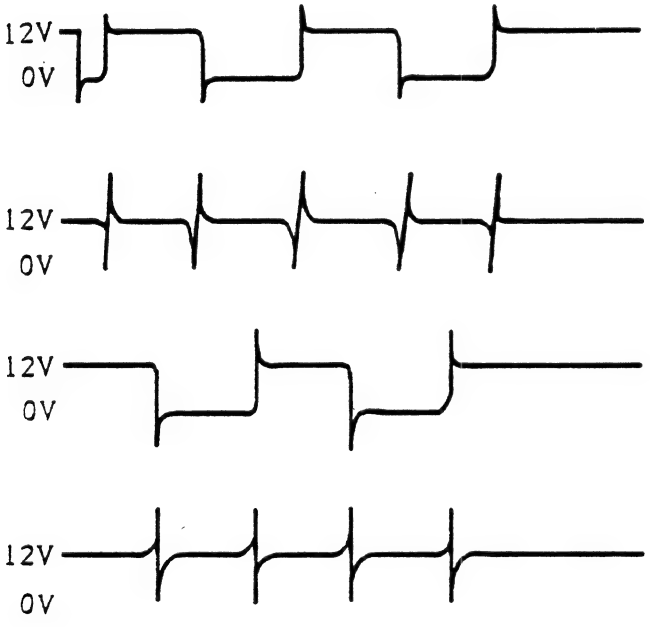
When speed pot VR2 is adjusted, the voltage on Pin 10 of U5 increases or decreases. This causes a corresponding increase or decrease in the frequency of the AC signal on the motor control lines, Pin 8 of U5 and Pins 11 and 5 of U5.

## STEPPER DRIVE SIGNALS




NS01
NS02
NS03
NS04

Schematics
Pg. 5-7




Pin 3 of U2
Pin 6 of U2
Pin 3 of U3
Pin 6 of U3

Schematics
Pg. 5-7

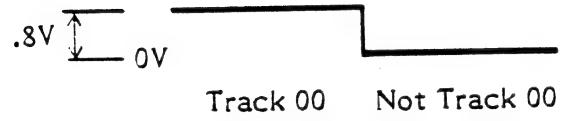
Pin 5 of U2 and U3 is + 12V DC.

## DISKETTE ENABLE SIGNAL

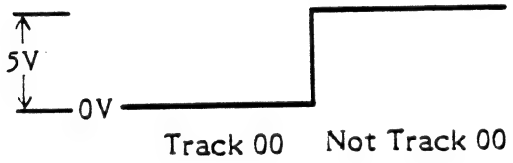
| Enabled | Disabled |
|---|---|
| (IC U6)<br>Pin 10 = 0V<br>Pin 12 = 5V<br>Pin 8 = 4.5V | (IC U6)<br>Pin 10 = 5V<br>Pin 12 = 0V<br>Pin 8 = 0V |

Schematics, Pg. 5-7

## TRACK 00 SIGNAL

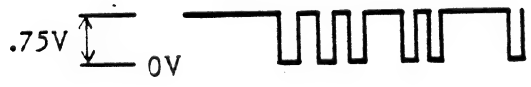



Base of Q5
Schematics, Pg. 5-7

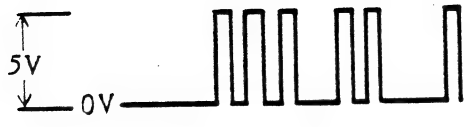



Collector of Q5
Schematics, Pg. 5-7

## DATA - IN SIGNAL

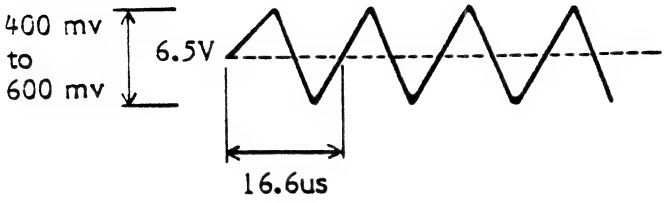



Pin 2 of U1
Schematics, Pg. 5-9



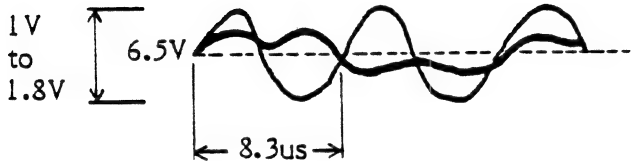

Pin 1 of U1
Schematics, Pg. 5-9

## READ SIGNALS



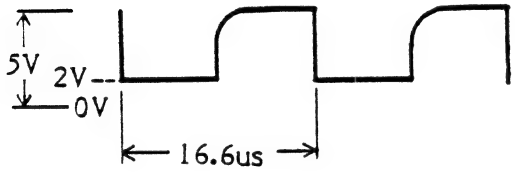

TP1 or TP2

Schematics, Pg. 5-3



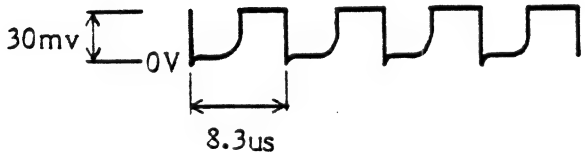

TP3 or TP4

Schematics, Pg. 5-3



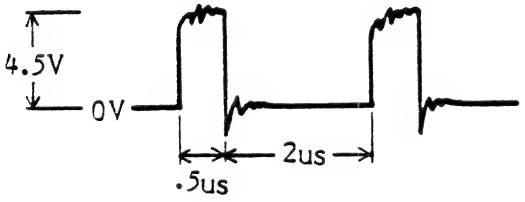

TP5

Schematics, Pg. 5-3




TP16

Schematics, Pg. 5-3



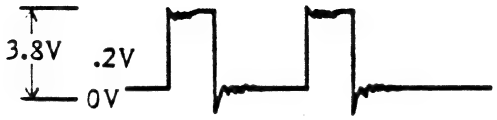

TP6

Schematics, Pg. 5-3

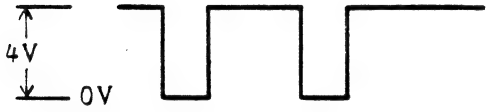

Pin 27 of U13

Schematics, Pg. 5-5

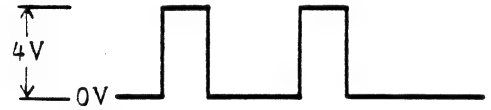
## WRITE SIGNALS



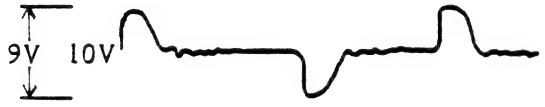

TP11
Schematics, Pg. 5-5




Pin 9 of U18
Schematics, Pg. 5-3



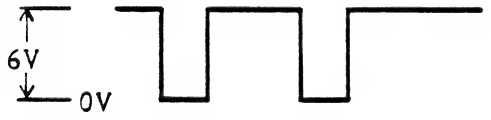

Pin 8 of U18
Schematics, Pg. 5-3




Pin 5 of U21


Pin 1 of U21
Schematics, Pg. 5-3

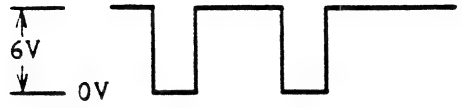
## WRITE GATE SIGNALS




Pin 10 of U16
Schematics, Pg. 5-5

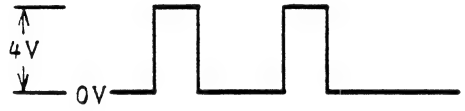

Pin 9 of U21
Schematics, Pg. 5-3

## ERASE GATE SIGNAL

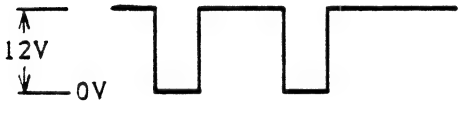



Pin 10 of U16
Schematics, Pg. 5-5


Pin 5 of U15
Schematics, Pg. 5-7



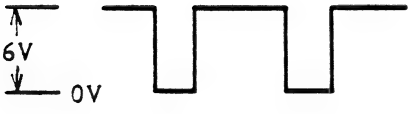

Pin 13 of U15
Schematics, Pg. 5-7




Pin 8 of U21
Schematics, Pg. 5-3


Collector of Q1
Schematics, Pg. 5-3

## ERASE SIGNAL



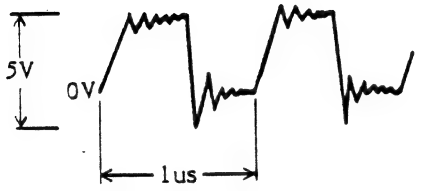

Pin 1 of U11
Schematics, Pg. 5-5


Pin 10 or 12 of U17
Schematics, Pg. 5-3

## CLOCK SIGNALS

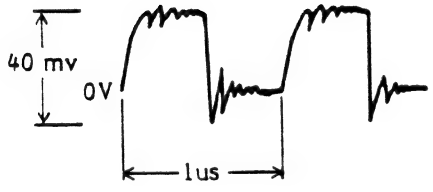

Pin 13 of U16
Schematics, Pg. 5-5

4 MHz Clock




Pin 5 of U14
Schematics, Pg. 5-5

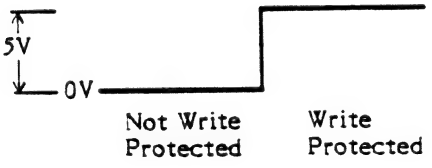
1 MHz Clock



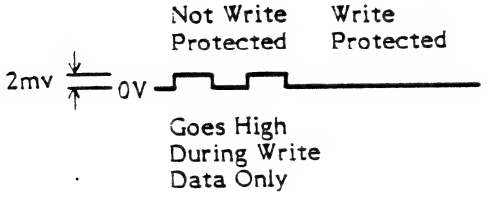

Pin 6 of U6
Schematics, Pg. 5-5

Phase 0 Clock

## WRITE PROTECT SIGNAL



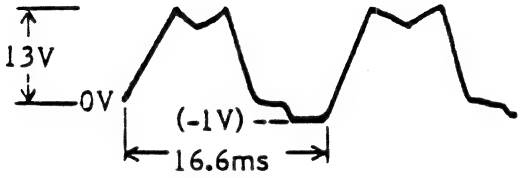

Pin 11 of U11
Schematics, Pg. 5-7



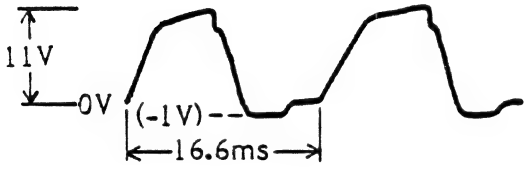

Pin 13 of U11
Schematics, Pg. 5-7

## POWER SUPPLY SIGNALS (AC)

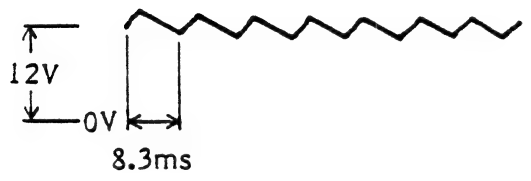
Schematics, Pg. 5-9




Cathode of CR20

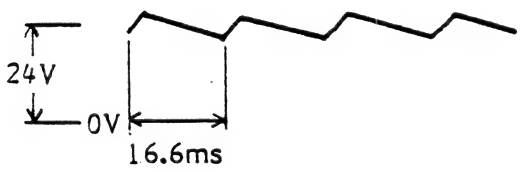



Cathode of CR19




Cathode of CR18


Cathode of CR15




Cathode of CR16

Anode of CR21 = 1.7V DC

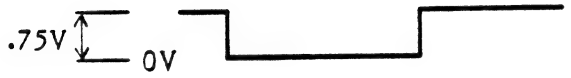
TP 13 = +5V DC
TP 14 = +12V DC
TP 15 = Ground

## DATA-OUT SIGNAL

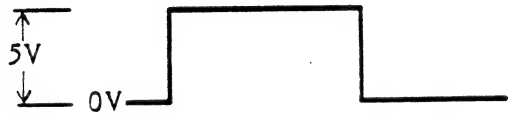

Pin 9 of U1
Schematics, Pg. 5-9


Pin 14 of U1
Schematics, Pg. 5-9

## COMMAND SIGNAL



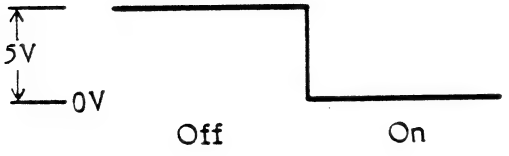

Pin 4 of U1
Schematics, Pg. 5-9




Pin 5 of U1
Schematics, Pg. 5-9

## VCC READY SIGNAL


Pin 6 of U1
Schematics, Pg. 5-9




Pin 8 of U1
Schematics, Pg. 5-9

## SECTION 5

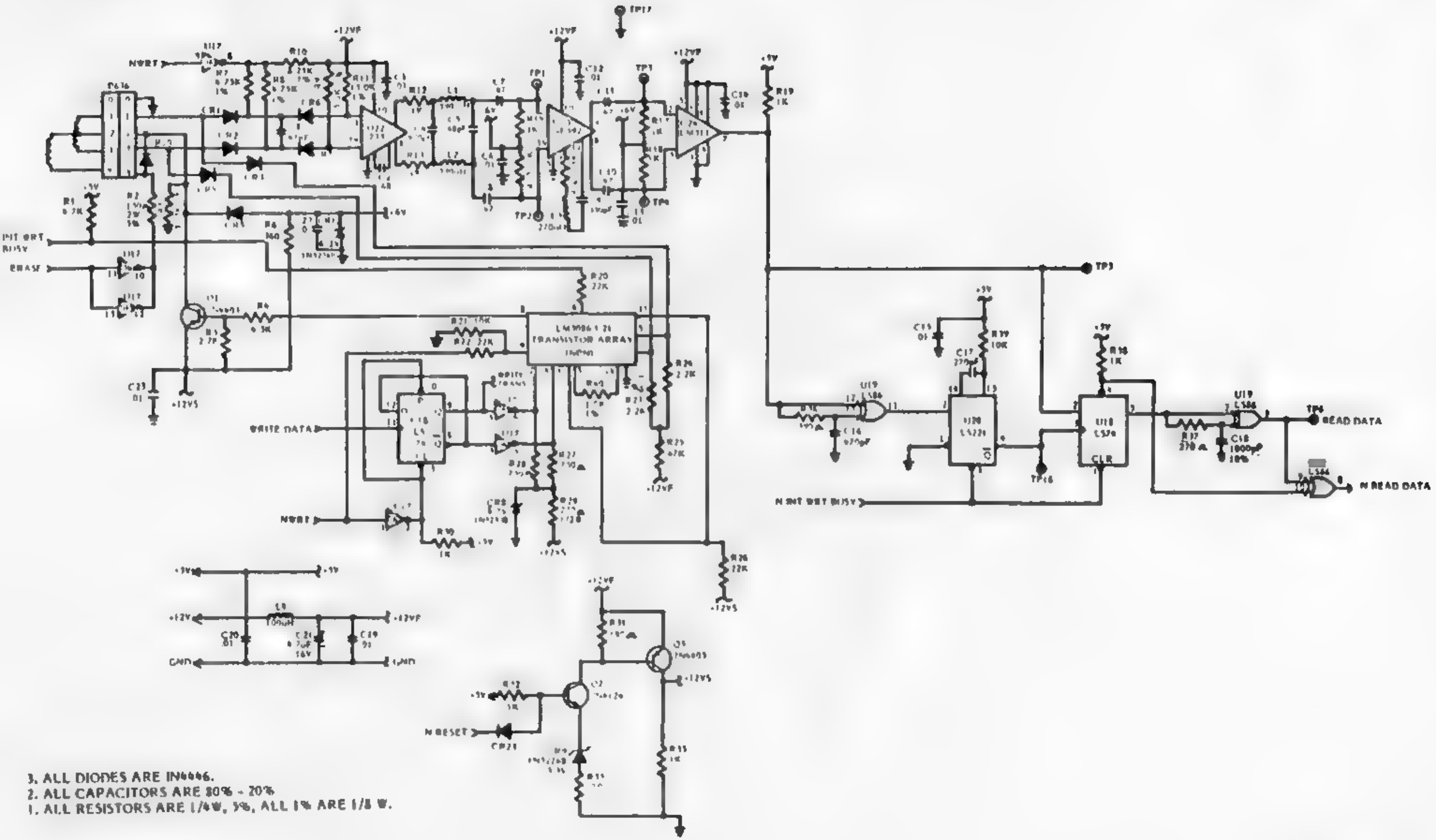
## ASSEMBLY DRAWINGS AND PARTS LIST

This section contains Schematics, Silkscreens and Parts List for the Atari 1050 Disk Drive.

Remove drawings from front of manual and insert them directly behind this page.

## 1050 PARTS LIST
## (TANDON)

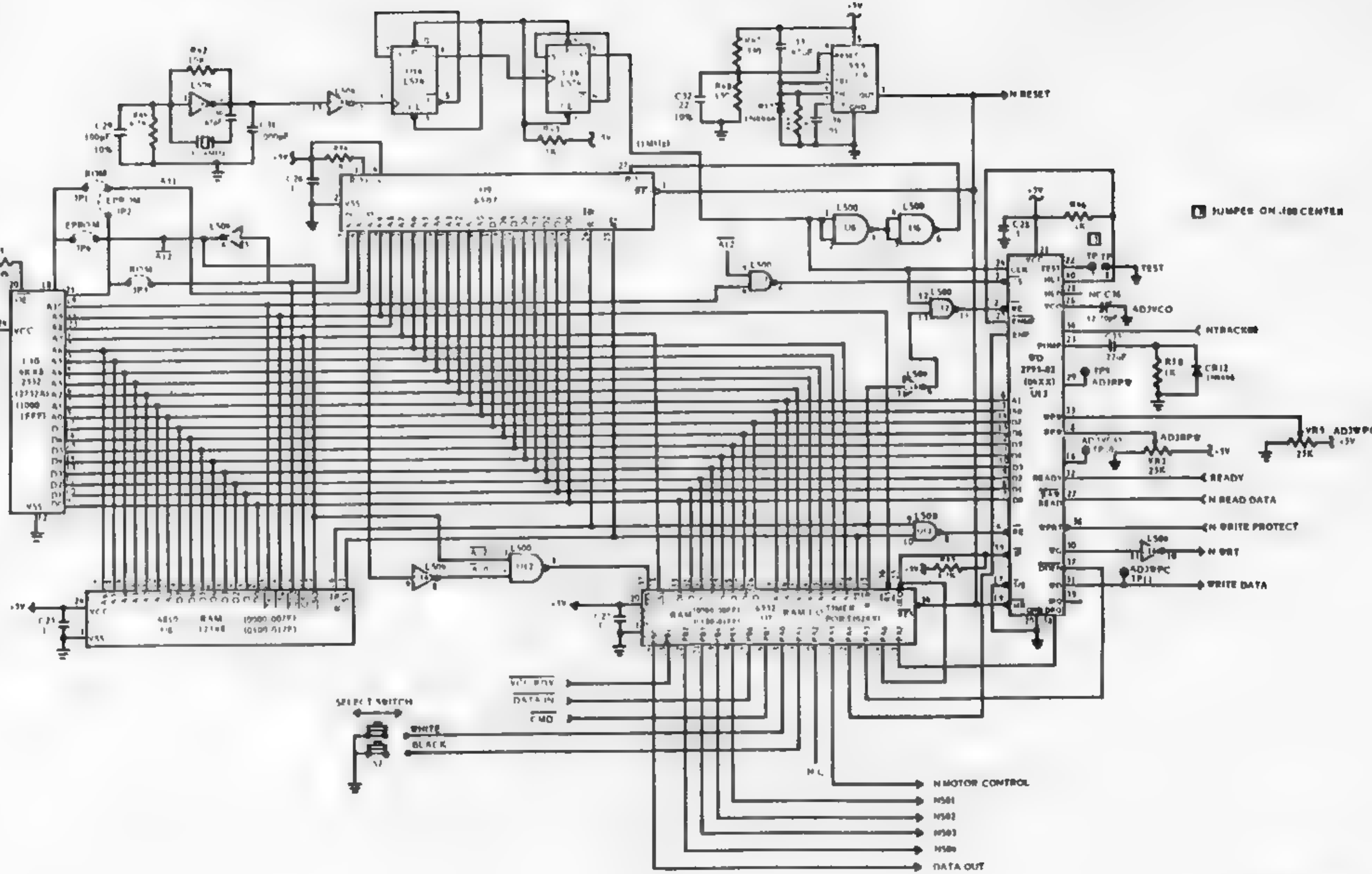
| LOCATOR | DESCRIPTION | PART NUMBER |
|---|---|---|
| | TM50-1 Drive Mech (Tandon) | FA100514 |
| | Enclosure, Top | FC100515 |
| | Enclosure, Bottom | FC100516 |
| | Front Bezel | FC100517 |
| | Photo Sensor | FC100518 |
| | Ready Sw. Assy. | FA100519 |
| | Spindle Motor | FC100520 |
| | **1050 PCB Assy.** | **FA100513** |
| L3 | Inductor, 270uH | FC100521 |
| L1,2 | Inductor, 390uH | FC100522 |
| R2 | Resistor, 150 Ohm, 2W | FC100524 |
| VR2 | Pot, Cermet, 2K | FC100525 |
| VR3,5 | Pot, Cermet, 25K | FC100526 |
| Q2,4,5 | Transistor, 2N4124 | FC100527 |
| Q1,3 | Transistor, 2N4403 | FC100528 |
| Q6 | Transistor, TIP110 | FC100529 |
| CR1-7,10,12,13 | Diode, 1N4446 | FC100530 |
| CR11 | Zener, 1N5224B, 6.2V | FC100531 |
| CR9 | Zener, 1N5226B, 3.3V | FC100532 |
| CR8 | Zener,1N5230B, 4.7V | FC100533 |
| Y1 | Crystal 4MHz | FC100534 |
| U15 | 74LS123, I.C. | FC100535 |
| U5 | LM2917, I.C. | C017101 |
| U2,3 | 75478, I.C. | FC100536 |
| C36 | Cap, Variable, 12-70pF | FC100543 |
| U22 | LM733, I.C. | FC100537 |
| U23 | NE592, I.C. | C017951 |
| U24 | LM311, I.C. | C014332 |
| U17 | SN7406, I.C. | FC100538 |
| U19 | 74LS86, I.C. | 37-74LS86 |
| U20 | 74LS221, I.C. | FC100540 |
| U14,18 | 74LS74, I.C. | C016045 |
| U1,21 | LM3086, I.C. | C016821 |
| U6,U12 | 74LS00, I.C. | C014341 |
| U11 | 74LS02, I.C. | C014340 |
| U16 | 74LS04, I.C. | C017096 |
| U4 | LM555, I.C. | C019748 |
| U10 | ROM, Custom 2732, I.C. | FC100541 |
| U8 | RAM, 6810 (1MHz), I.C. | C014328 |
| U9 | MPU, 6507 (1MHz), I.C. | C010745 |
| U13 | FDC WD2793-02, I.C. | FC100542 |
| U7 | PIA, 6532, I.C. | C010750 |
| CR17-20 | Diode, MR501 | C014398 |




3. ALL DIODES ARE IN4446.
2. ALL CAPACITORS ARE 80% - 20%
1. ALL RESISTORS ARE 1/4W, 5%, ALL 1% ARE 1/8 W.

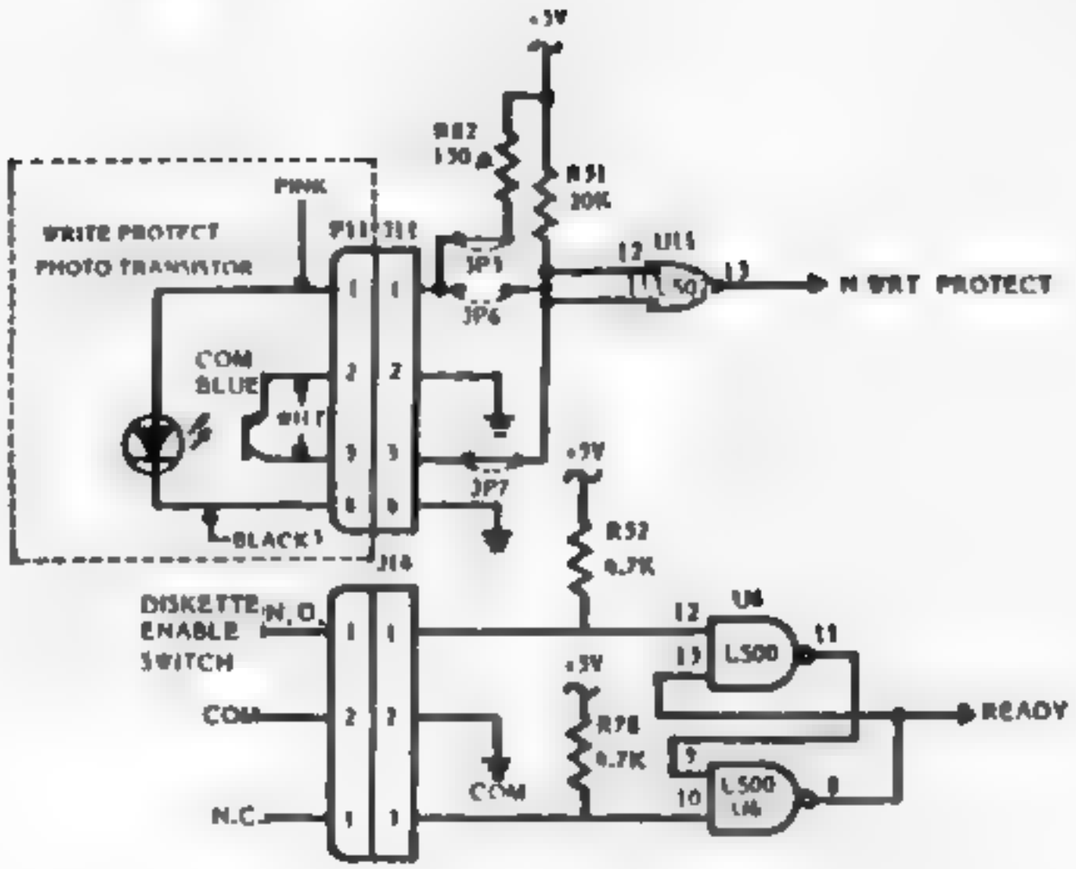


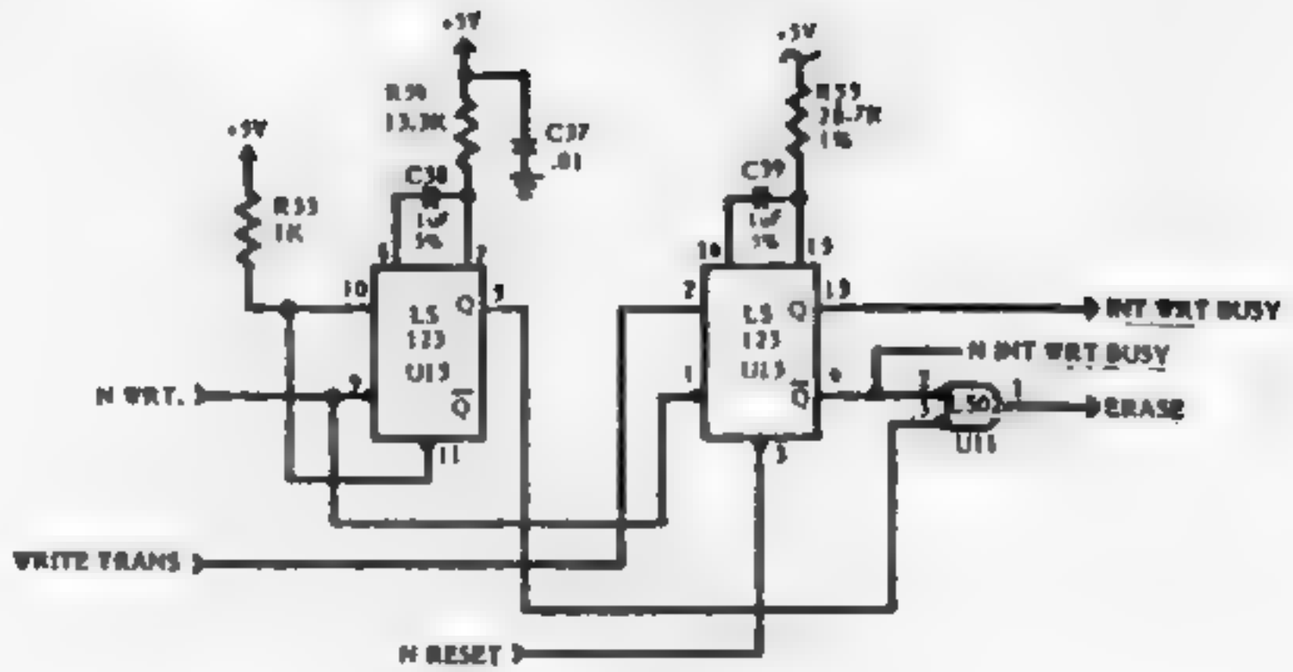
1050 Schematic
(Tandon) 1 of 4

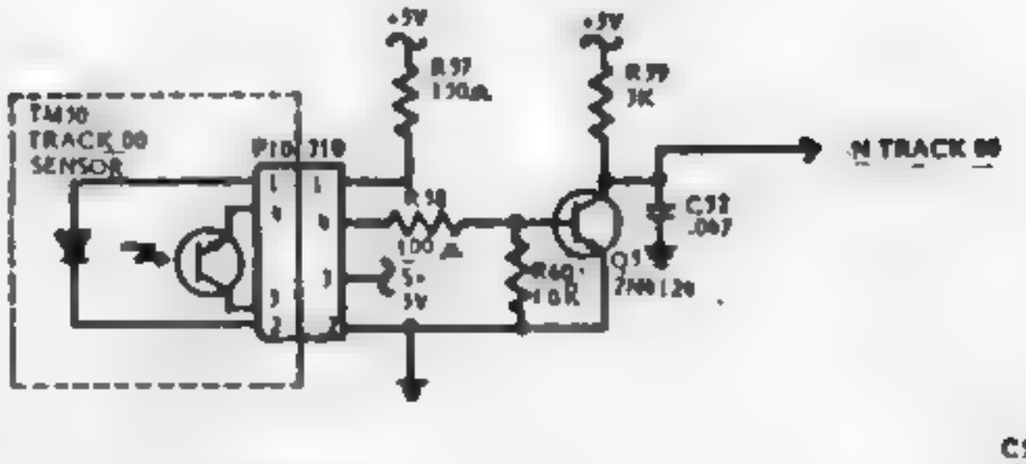


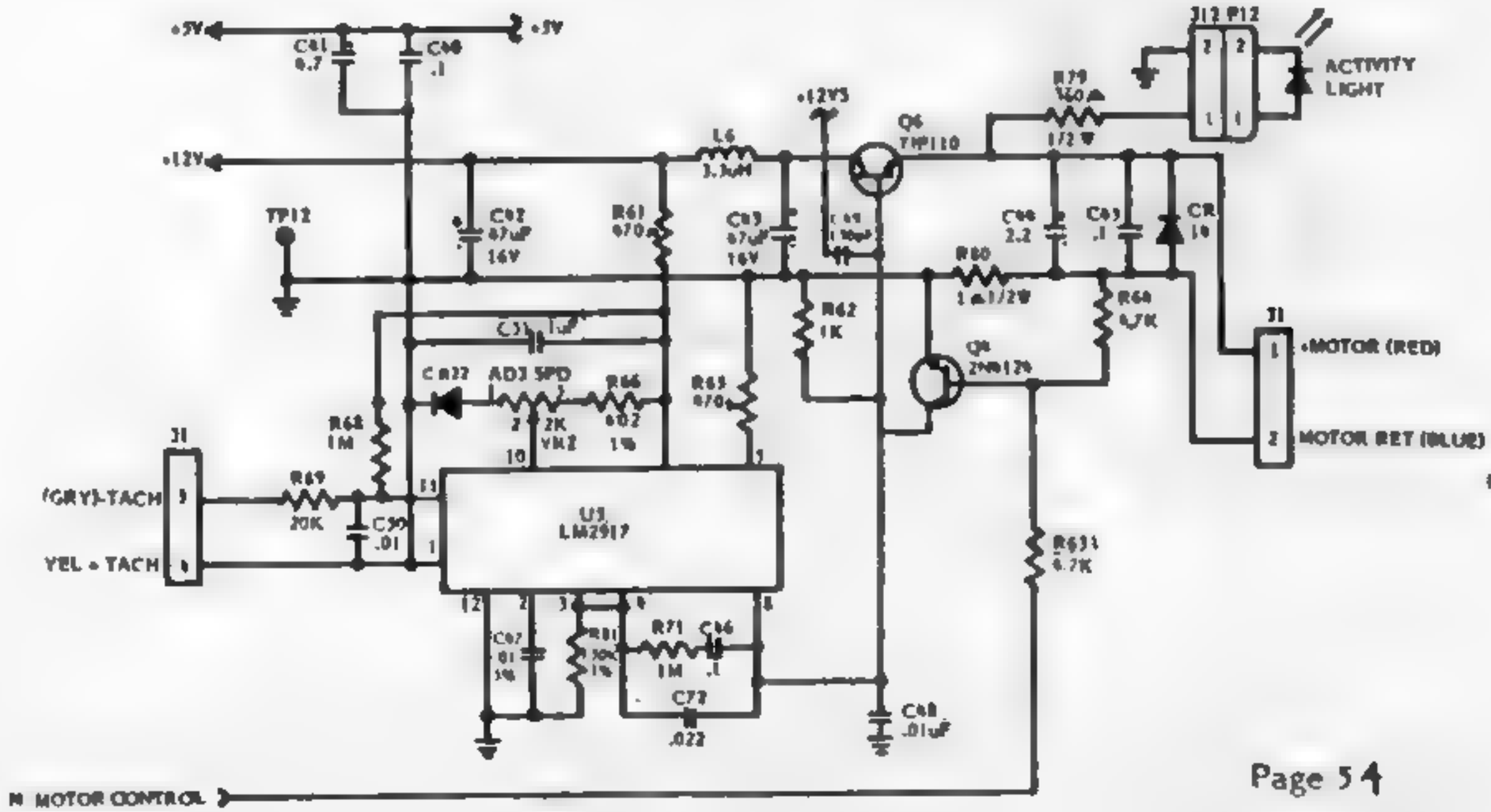


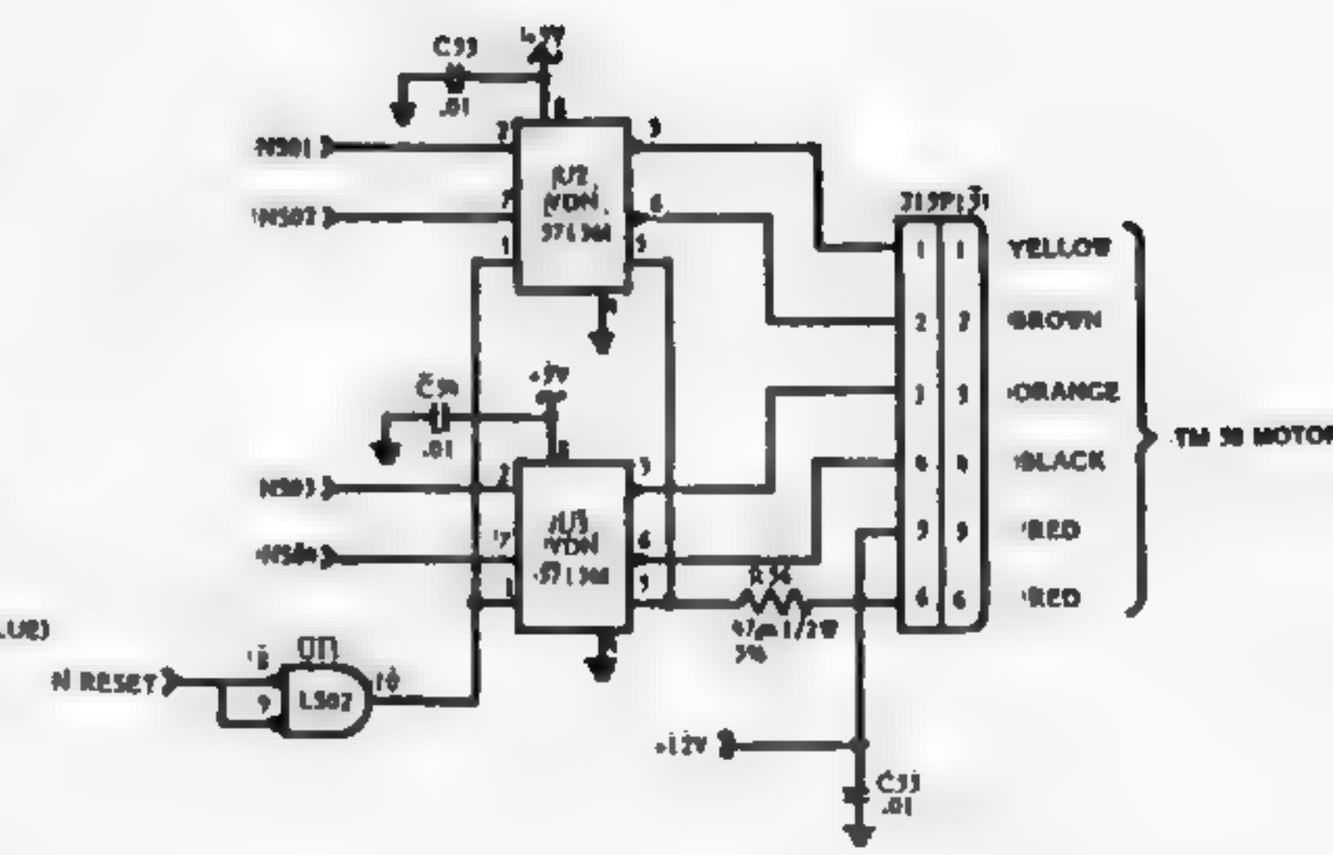

1050 Shematic
(Tandon) 2 of 4



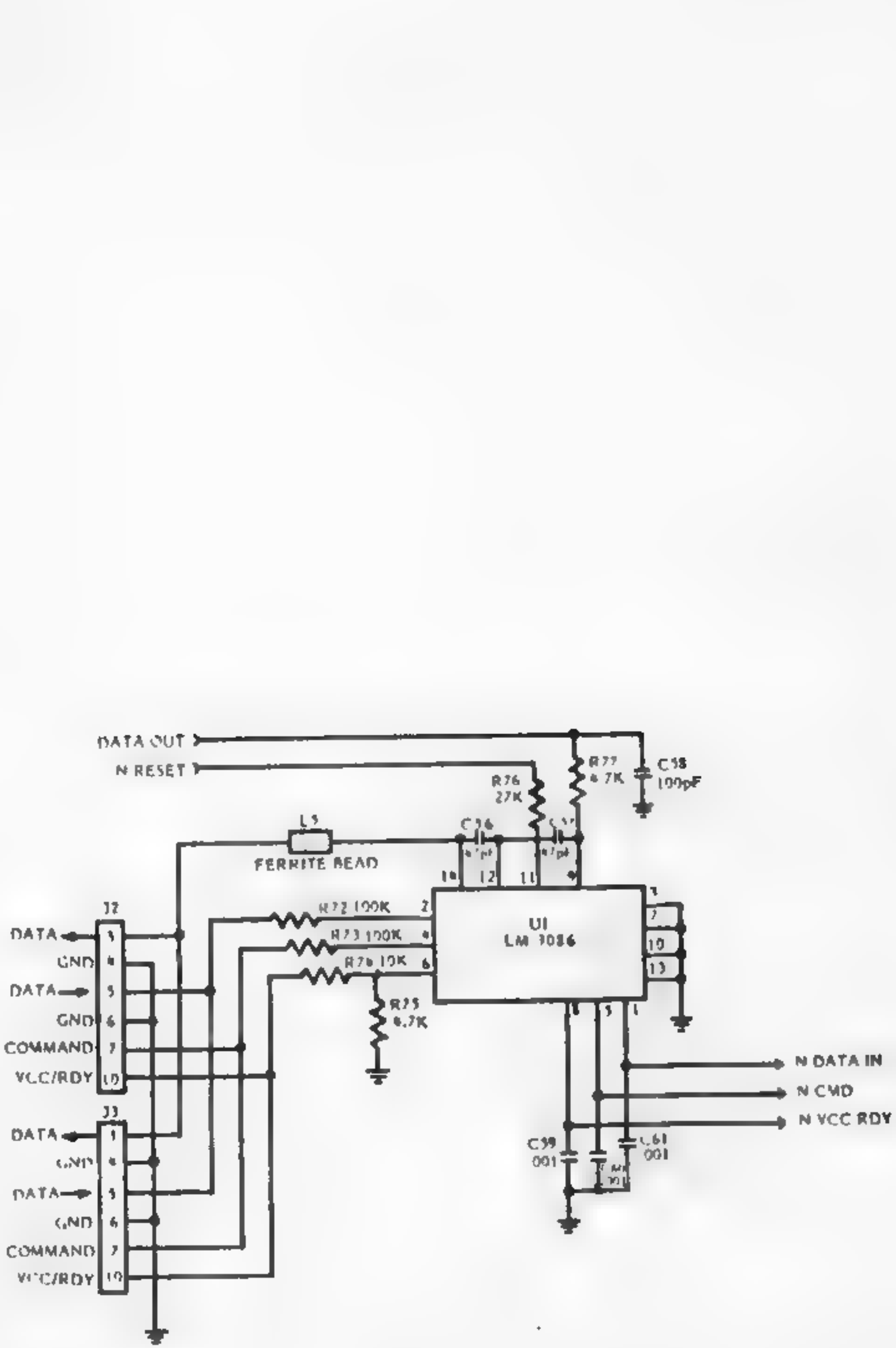



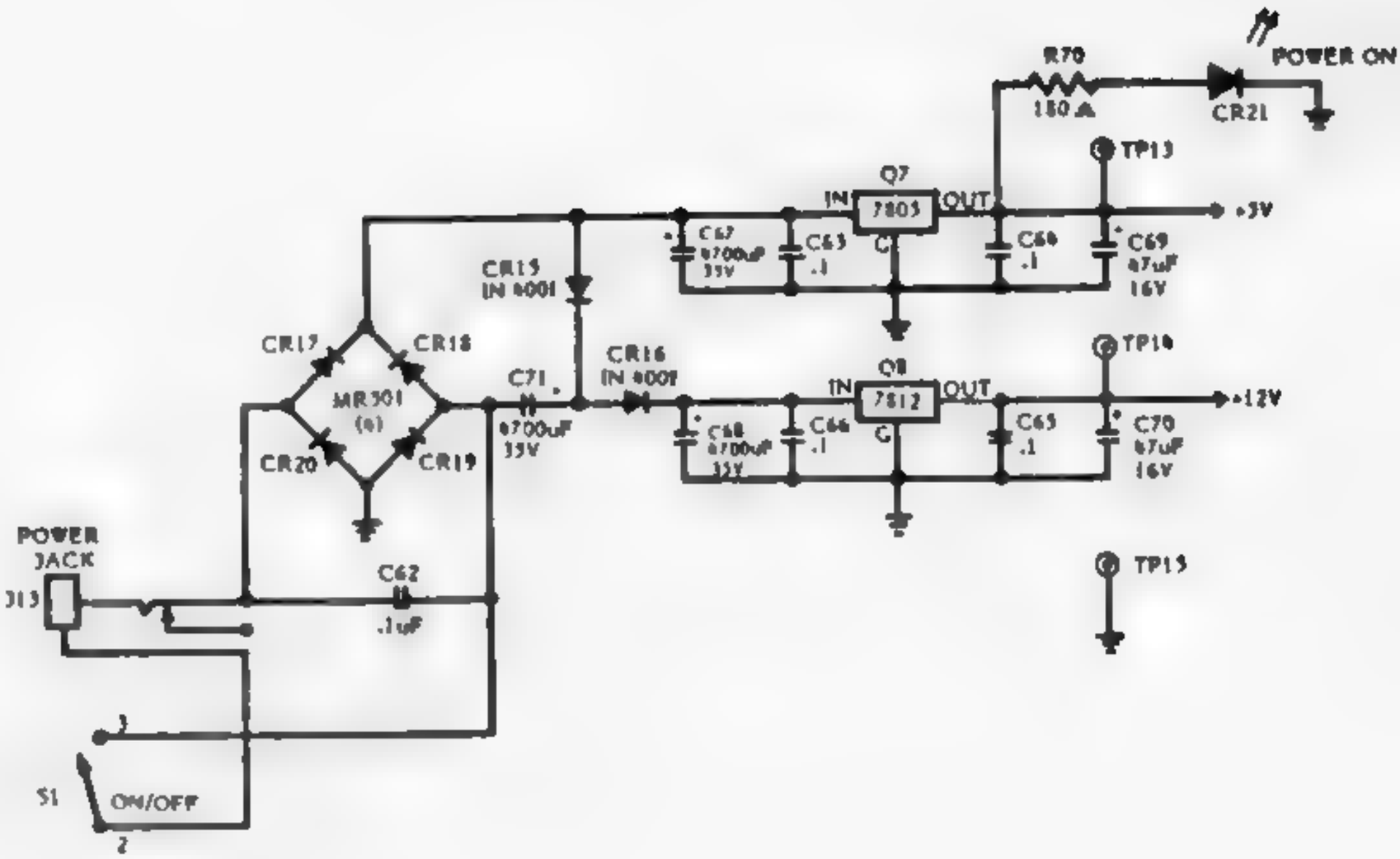





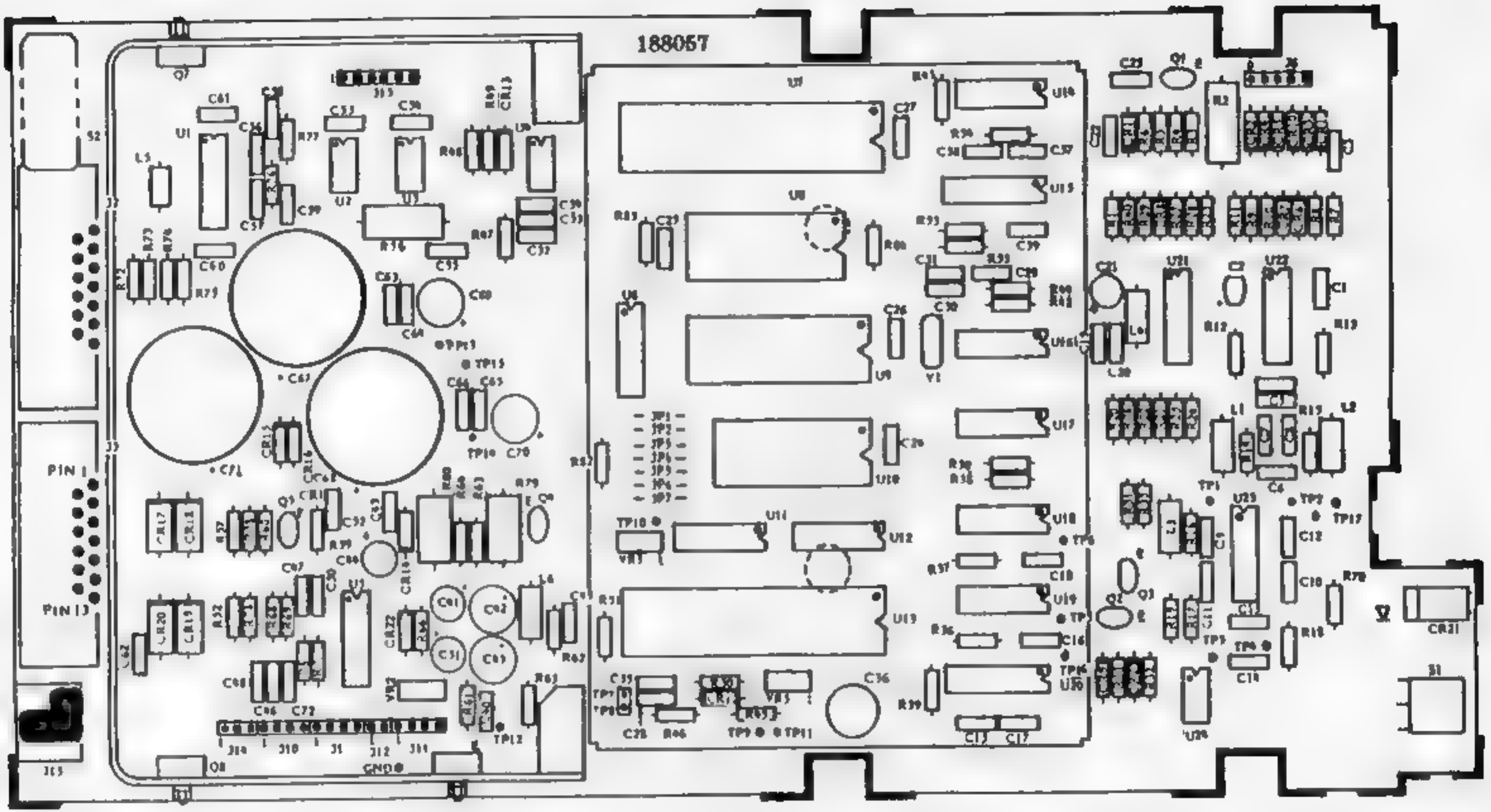

1050 Schematic
(Tandon) 3 of 4





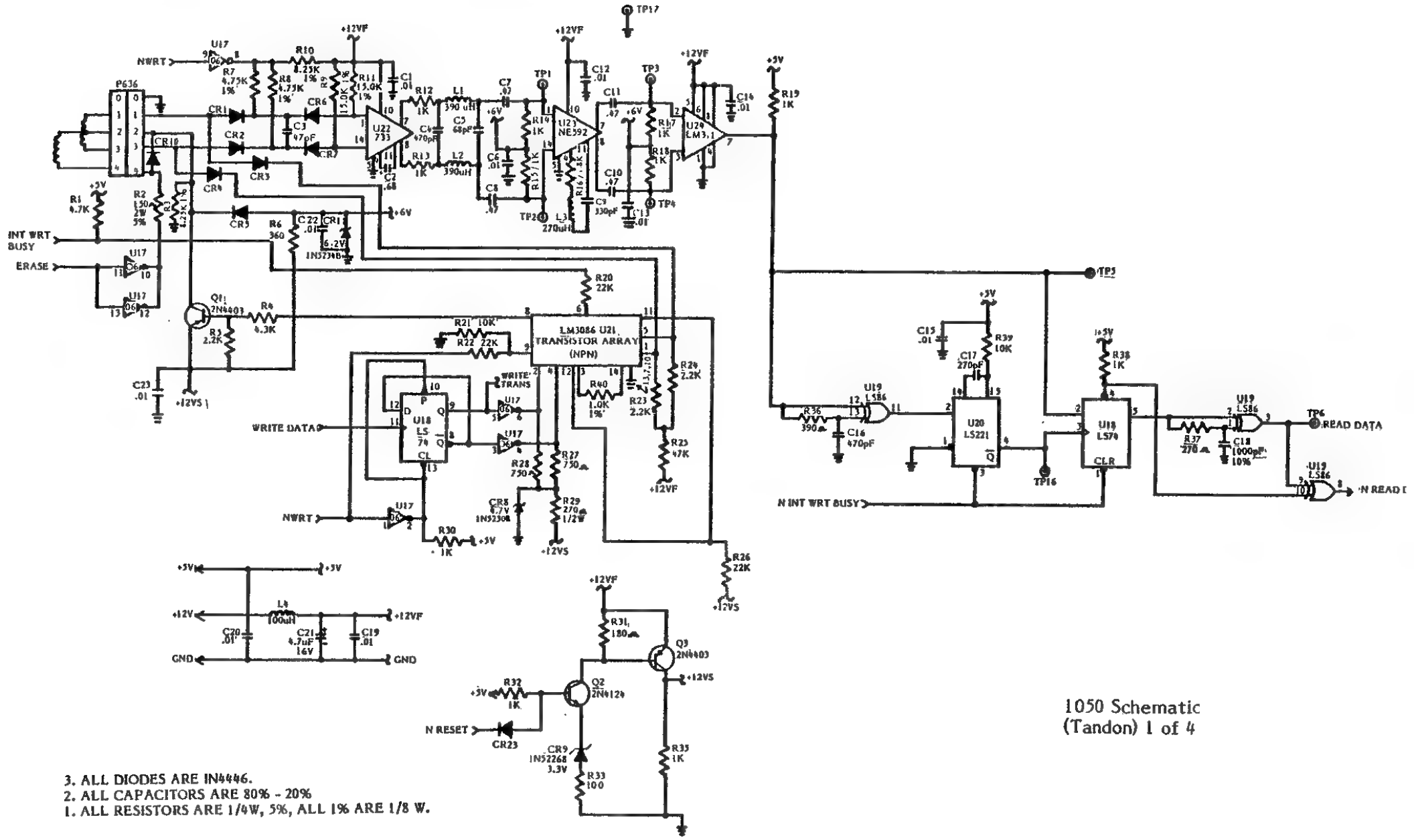

1050 Schematic
(Tandon) 4 of 4




JUMPER TABLE

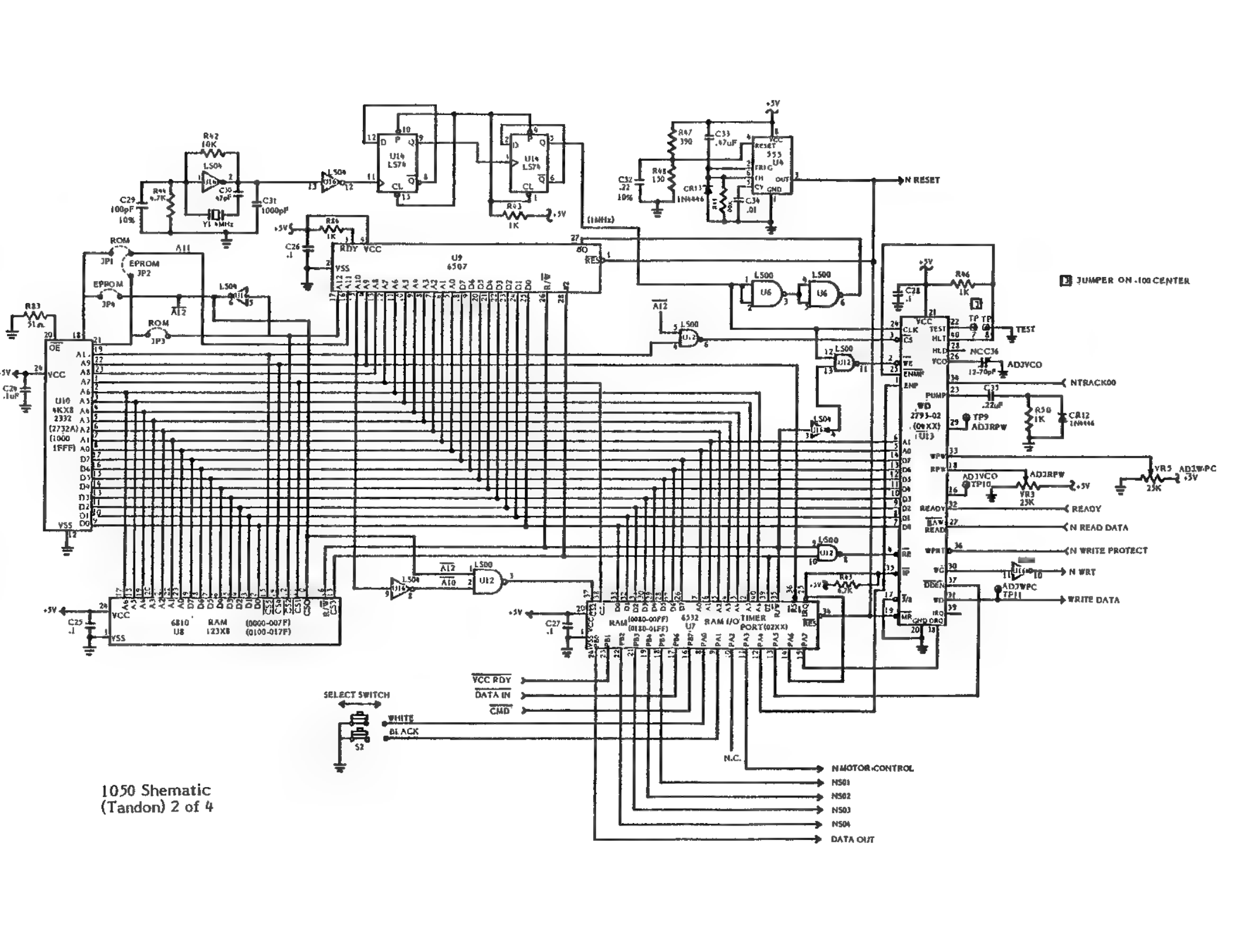
| Write Protect - Optical | EPROM | ROM |
|---|---|---|
| JP5 | JP2 | JP1 |
| JP7 | JP4 | JP3 |

1050 Silkscreen

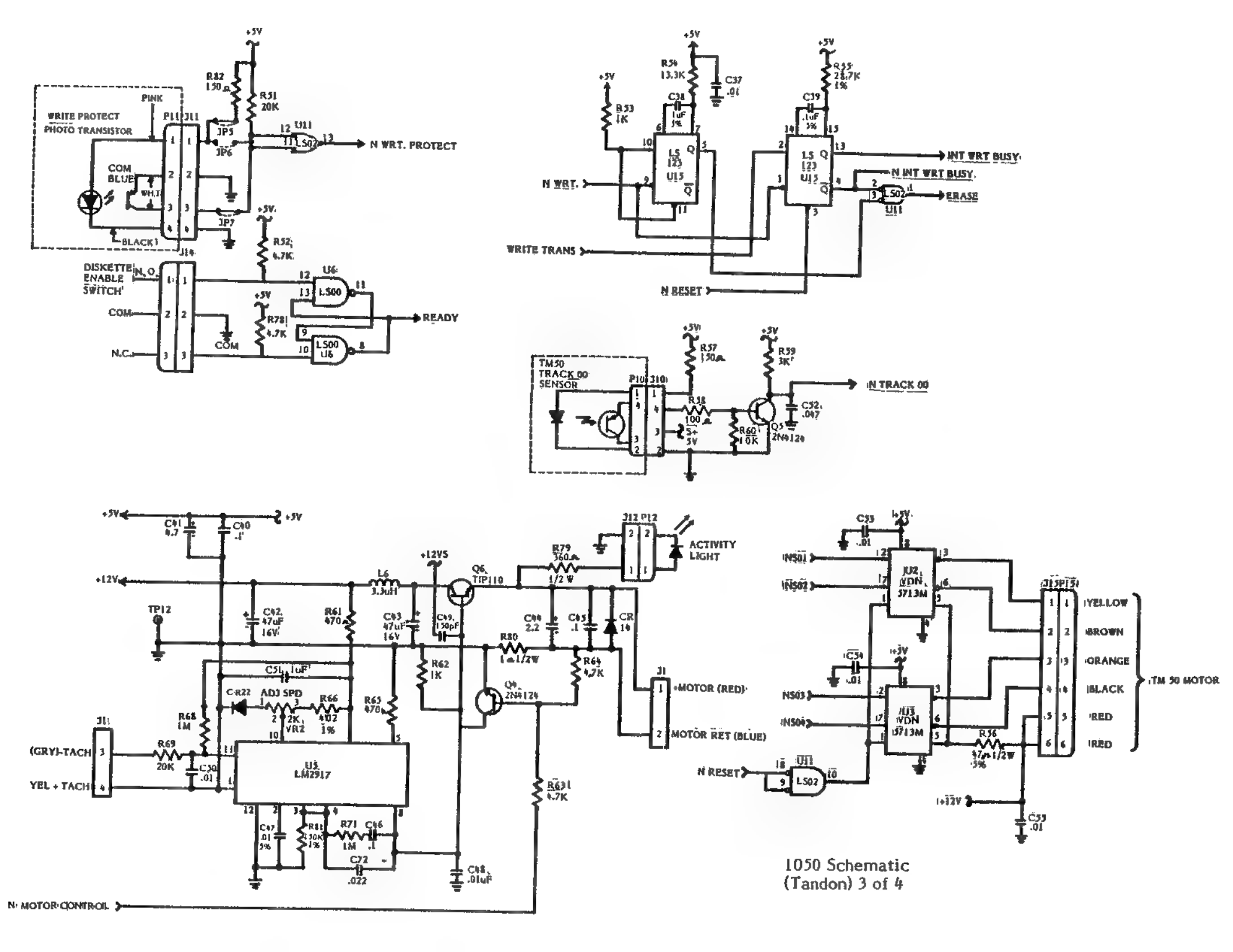



1050 Schematic
(Tandon) 1 of 4

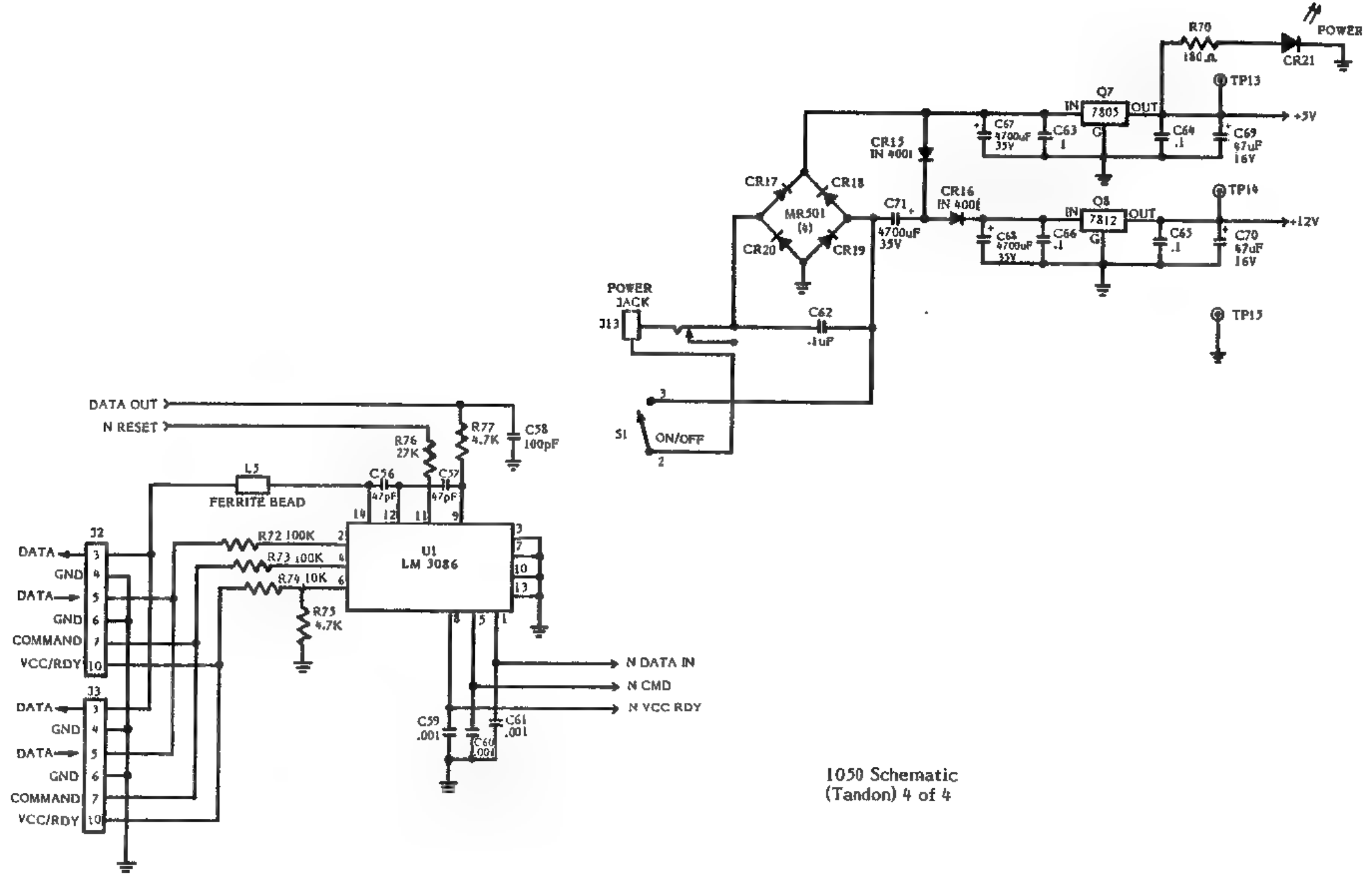
3. ALL DIODES ARE IN4446.
2. ALL CAPACITORS ARE 80% - 20%
1. ALL RESISTORS ARE 1/4W, 5%, ALL 1% ARE 1/8 W.



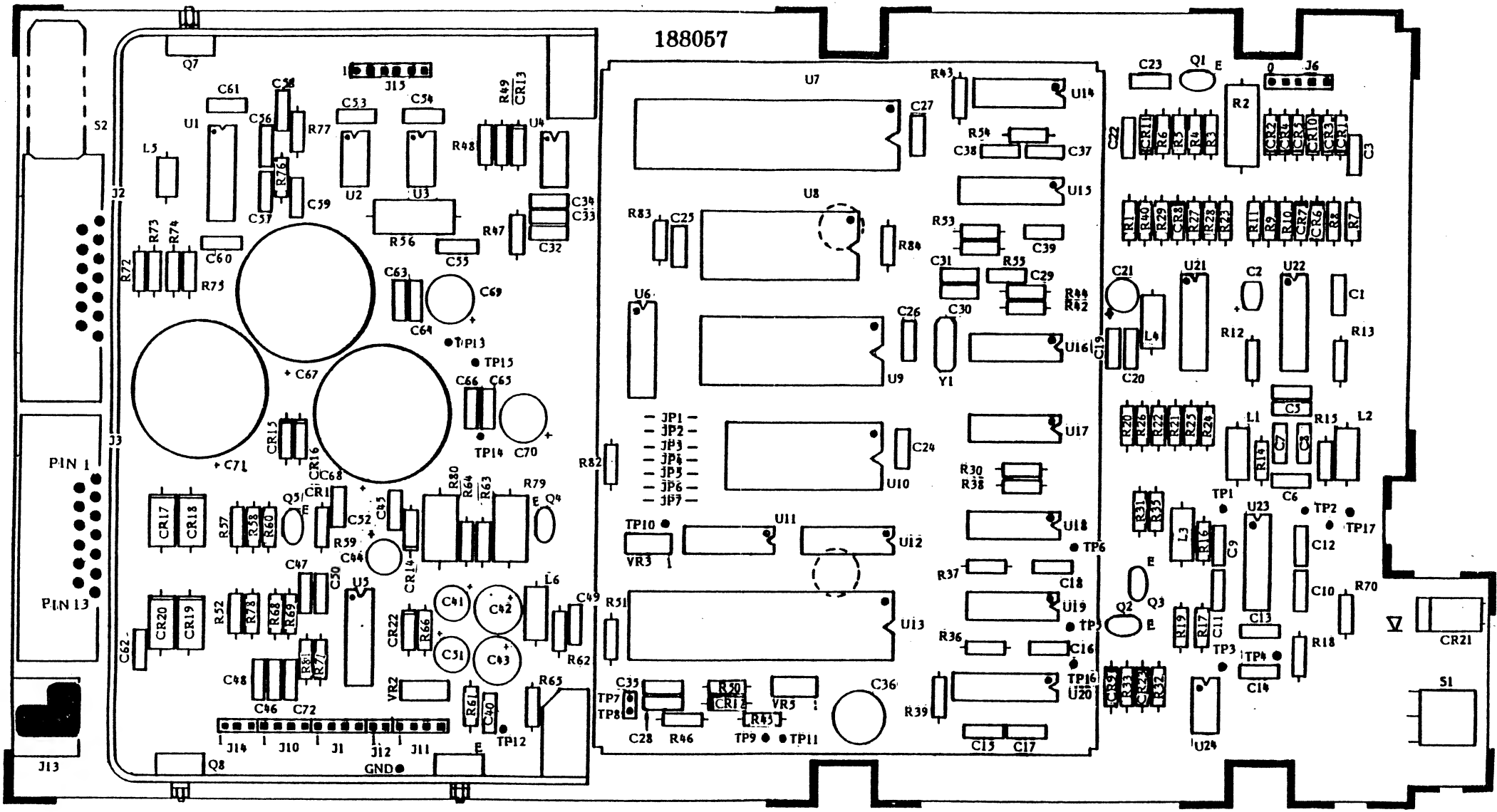

1050 Shematic
(Tandon) 2 of 4




1050 Schematic
(Tandon) 3 of 4




1050 Schematic
(Tandon) 4 of 4




JUMPER TABLE

| Write Protect - Optical | EPROM | ROM |
|---|---|---|
| JP5 | JP2 | JP1 |
| JP7 | JP4 | JP3 |

1050 Silkscreen

## APPENDIX 6A

## 1050 SPECIFICATIONS

### Functional Specification

Key Features

- o Lower Cost than 810
- o Fully compatible with 810 in single density (FM) mode.
- o Double Density read/write operation using (MFM) encoding
- o Fully compatible with existing Atari disk operating system
- o Fully support the Atari SIO interface and protocol
- o Support new high level macro command requested by next generation Atari disk operating system

Disk Drive Specification

| | Single Density (Read/Write) | Double Density (Read/Write) |
|---|---|---|
| Tracks Per Surface | 40 | 40 |
| Tracks Per Inch | 48 | 48 |
| Recording Density (Track 39, Max) | 2,878 BPI | 5,757 BPI |
| Flux Density (Track 39, Max) | 5,757 FCI | 5,757 FCI |
| Encoding Method | FM | MFM |
| Capacity | | |
| Unformatted | | |
| Per Track | 3,382 Bytes | 6,510 Bytes |
| Per Surface | 135,280 Bytes | 260,400 Bytes |
| Formatted | | |
| Sectors/Track | 18 | 26 |
| Bytes/Per Sector | 128 Bytes | 128 Bytes |
| Bytes/Per Track | 18 X 128 Bytes | 26 X 128 Bytes |
| Bytes/Per Surface | 92,160 Bytes | 133,120 Bytes |
| Transfer Rate | 125,000 BPS | 250,000 BPS |

| | Single Density (Read/Write) | Double Density (Read/Write) |
|---|---|---|
| Read/Write Head | 1 | 1 |
| Write Protect Sensor | YES | YES |
| Track 00 Sensor | YES | YES |
| Rotational Speed | 288 RPM | 288 RPM |
| Rotational Speed Accuracy | + - 3% | + - 3% |
| Average Latency | 110 MS | 110 MS |
| Access Time | | |
| Track to Track (MAX) | 40 MS | 40 MS |
| Head Settling (MAX) | 30 MS | 30 MS |
| Motor Start (MAX) | 1000 MS | 1000 MS |

Media Requirements

Single Density

Soft Sectored, per Atari Specification (#C016884)

Double Density

Soft Sectored, per Atari Specification (#C016890)

Physical and Dimensional Specification

Drive outside dimension (Exclusive of front panel)

| | |
|---|---|
| HEIGHT | 1.70 Inches (Max) |
| WIDTH | 6.00 Inches (MAX) |
| LENGTH | 8.00 Inches (MAX) |
| WEIGHT | 6 Pounds (Max) |

Electrical Specification

Drive Read/Write Electronics

| | |
|---|---|
| Head Voltage at 1F amplitude | 10 MV (Max) at Track 00 |
| Head Voltage at 2F Amplitude | 3 MV (MIN) at Track 39 |

*These data values should be obtainable from various diskette vendors.

Power Consumption

AC Power Adapter (North American Version)

Consult the Atari 31 VA AC Power Adapter Specification (#C017945)

AC Power Adapter (International Version) TBD

System Electronics

Including Drive Electronics, Controller Electronics and Power Supply Electronics

| | |
|---|---|
| Input Voltage | 8.52V AC +-12% @ 60 +-3Hz |
| Power Consumption | |
| Standby | 15 Watts (MAX) |
| Operating | 30 Watts (MAX) |
| Start Up | 50 Watts (MAX) |

ATARI

**Consumer Product Service**
**Manager of Technical Support**

# TECH TIP

TT
HCD
number 21

| MODEL: Atari 1050 Disk Drive | DATE: September 30, 1983 |
|---|---|

**SUBJECT:**

Consumers may experience problems booting some non-Atari software due to protection schemes used.

**DESCRIPTION:**

Some third party software programs will either not boot or not run on the 1050 Disk Drive. These same programs will boot on an 810 disk drive.

**PROBLEM:**

The first 1700 units released to the field have a revision "E" or "F" EPROM installed. This revision of the firmware returns a different error status than the 810 disk drive when certain types of protection schemes are used on the diskette.

**SOLUTION:**

Disassemble the 1050 disk drive and check for Rev. "E" or "F" EPROM at location U10. Replace this EPROM with a FC100541 Rev. 1 on the PCBA. Reassemble and perform a functional test of the unit, consisting of the following, until the 1050 service manual is released.

Boot a DOS 2.0 Master Diskette

Format a scratch diskette and write "DOS" files to it

**ADDITIONAL INFORMATION:**

*** The Rev. "E" or "F" EPROM must be returned to Atari for reburning at FC100541, Rev. 1. ***

After removing the EPROM from the PCBA place it in the static free container the Rev. "J" EPROM was received in and return to Atari.

**PROBLEM REPORTING:**

If you have questions or require further explanation concerning this Tech Tip, contact your ATARI Tech-line Specialists:

Inside California
(800)672-1466

Outside California
(800) 538-1535